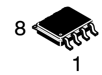
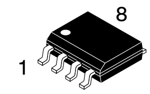
Serial Flash Memory 16 Mb (2048K x 8)

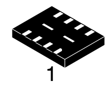
LE25S161



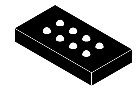
VSOIC8 NB
CASE 753AA



SOIC 8
CASE 751BD



UDFN8
CASE 506DC



WLCSP8
CASE 567YR

Overview

The LE25S161 is a SPI bus flash memory device with a 16 Mbit (2048K x 8−bit) configuration. It uses a single power supply. While making the most of the features inherent to a serial flash memory device, the LE25S161 is housed in an 8−pin ultra−miniature package. All these features make this device ideally suited to storing program in applications such as portable information devices, which are required to have increasingly more compact dimensions.

The LE25S161 also has a small sector erase capability which makes the device ideal for storing parameters or data that have fewer rewrite cycles and conventional EEPROMs cannot handle due to insufficient capacity.

Features

- Operations Power Supply: 1.65 to 1.95 V Supply Voltage Range
- Operating Frequency: 70 MHz (Max)
- Temperature Range: –40 to +90°C
- Serial Interface: SPI Mode 0, Mode 3 Supported
- Electronic Identification: JDEC ID, Device ID, Serial Flash Discoverable Parameter (SFDP)
- Sector Size: 4 kbytes/Small Sector, 64 kbytes/Sector
- Erase Functions: Small Sector Erase (SSE), Sector Erase (SE), Chip Erase (CHE)
- Page Program Function: 256 bytes/Page
- Status Functions: Ready/Busy Information, Protect Information
- Low Operation Current: 5.0 mA (Low−power Program Mode, Typ), 3.5 mA (Low−Power Read Mode, Typ)
- Erase Time: 10 ms (SSE, Typ), 15 ms (SE, Typ), 210 ms (CHE, Typ)
- Page Program Time (tPP): 0.4 ms/256 bytes (Typ.), 0.7 ms/256 bytes (Max.)
- Emergency Shutdown of the Current Consumption:
  Transition to a Standby State in Less than 20 μs from the Active by Write Suspend
  Transition to a Standby State in Less than 40 μs from the Active by Software Reset
- High Reliability: 100,000 Erase/Program Cycles
  20 Years Data Retention Period
- Package:
  LE25S161FDTWG VSOIC8 NB, CASE 753AA
  LE25S161MDTWG SOIC 8, 150 mils, CASE 751BD
  LE25S161PCTXG UDFN8 4 x 3, 0.8P, CASE 506DC
  LE25S161XBTAG WLCSP8, 2.92 x 1.53, CASE 567YR
  KGD

MARKING DIAGRAM

5S161
00
ALYW

5S16100 = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
Y = Year of Production
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
LE25S161FDTWG	VSOIC8 NB (Pb−Free / Halide Free)	3000 / Tape & Reel
LE25S161MDTWG	SOIC8 (Pb−Free / Halide Free)	2000 / Tape & Reel
LE25S161PCTXG	UDFN8 (Pb−Free / Halide Free)	2000 / Tape & Reel
LE25S161XBTAG	WLCSP8 (Pb−Free / Halide Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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PACKAGE TYPES AND PIN CONFIGURATIONS

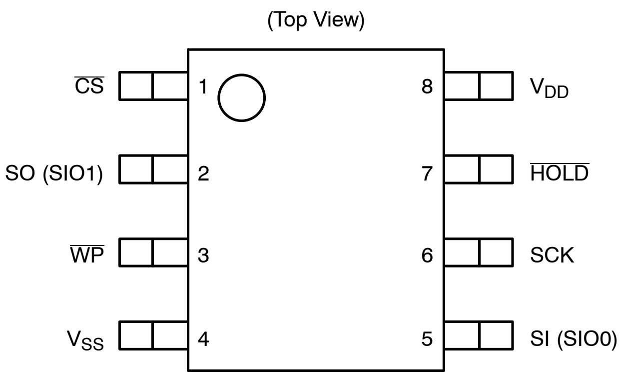


Figure 1. SOIC8 (LE25S161MDTWG) and VSOIC8 NB (LE25S161FDTWG)

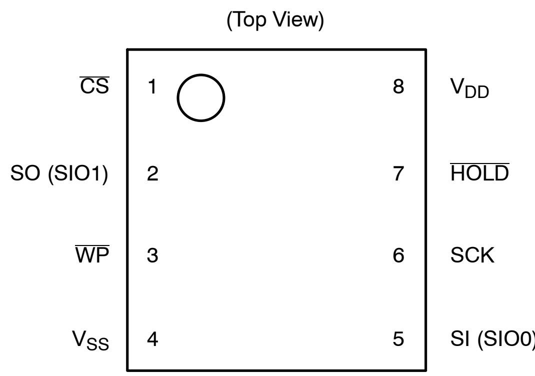


Figure 2. UDFN8 (LE25S161PCTXG)

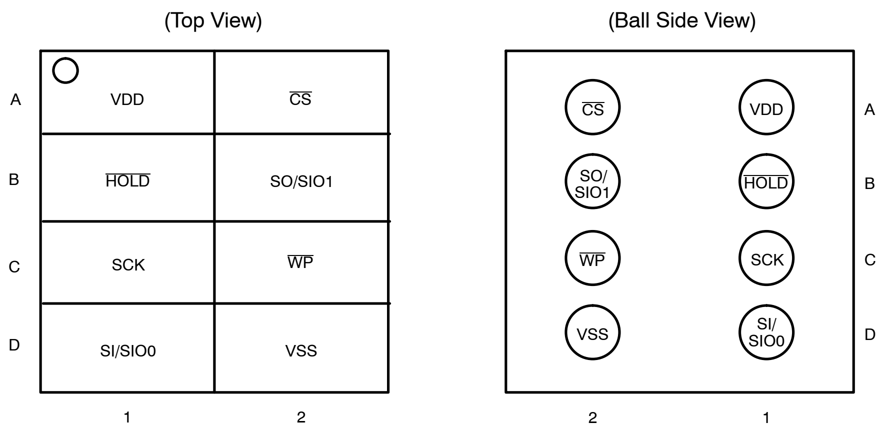


Figure 3. WLCSP8 (LE25S161XBTAG)

Table 1. PIN CONFIGURATION

Pad No.	Name
A2	$\overline{CS}$
B2	SO (SIO1)
C2	$\overline{WP}$
D2	V_{SS}
D1	SI (SIO0)
C1	SCK
B1	$\overline{HOLD}$
A1	V_{DD}

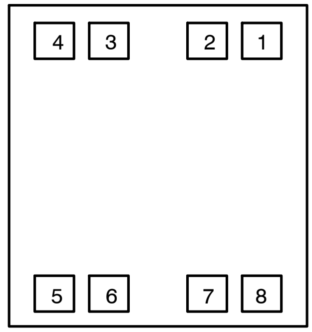


Figure 4. KGD

Table 2. PIN CONFIGURATION

Pad No.	Name
1	$\overline{CS}$
2	SO (SIO1)
3	$\overline{WP}$
4	V_{SS}
5	SI (SIO0)
6	SCK
7	$\overline{HOLD}$
8	V_{DD}

PIN DESCRIPTION

Table 3. PIN DESCRIPTION

Symbol	Pin Name	IIO	Description
$\overline{CS}$	Chip Select	I	The device becomes active when the logic level of this pin is low; it is deselected and placed in standby status when the logic level of the pin is high.
SCK	Serial Clock	I	This pin controls the data input/output timing. The input data and addresses are latched synchronized to the rising edge of the serial clock, and the data is output synchronized to the falling edge of the serial clock.
SI (SIO0)	Serial Data Input (Serial Data Input Output)	I/O	The data and addresses are input from this pin, and latched internally synchronized to the rising edge of the serial clock. (It changes into input/output pin during the Dual operation.)
SO (SIO1)	Serial Data Output (Serial Data Input Output)	I/O	The data stored inside the device is output from this pin synchronized to the falling edge of the serial clock. (It changes into input/output pin during the Dual operation.)
$\overline{WP}$	Write Protect	I	The Write Status Register Protect (SRWP) takes effect when the logic level of this pin is low.
$\overline{HOLD}$	Hold	I	Serial communication is suspended when the logic level of this pin is low.
V_{DD}	Power Supply		This pin supplies the 1.65 to 1.95 V supply voltage.
V_{SS}	Ground		This pin supplies the 0 V supply voltage.

BLOCK DIAGRAM

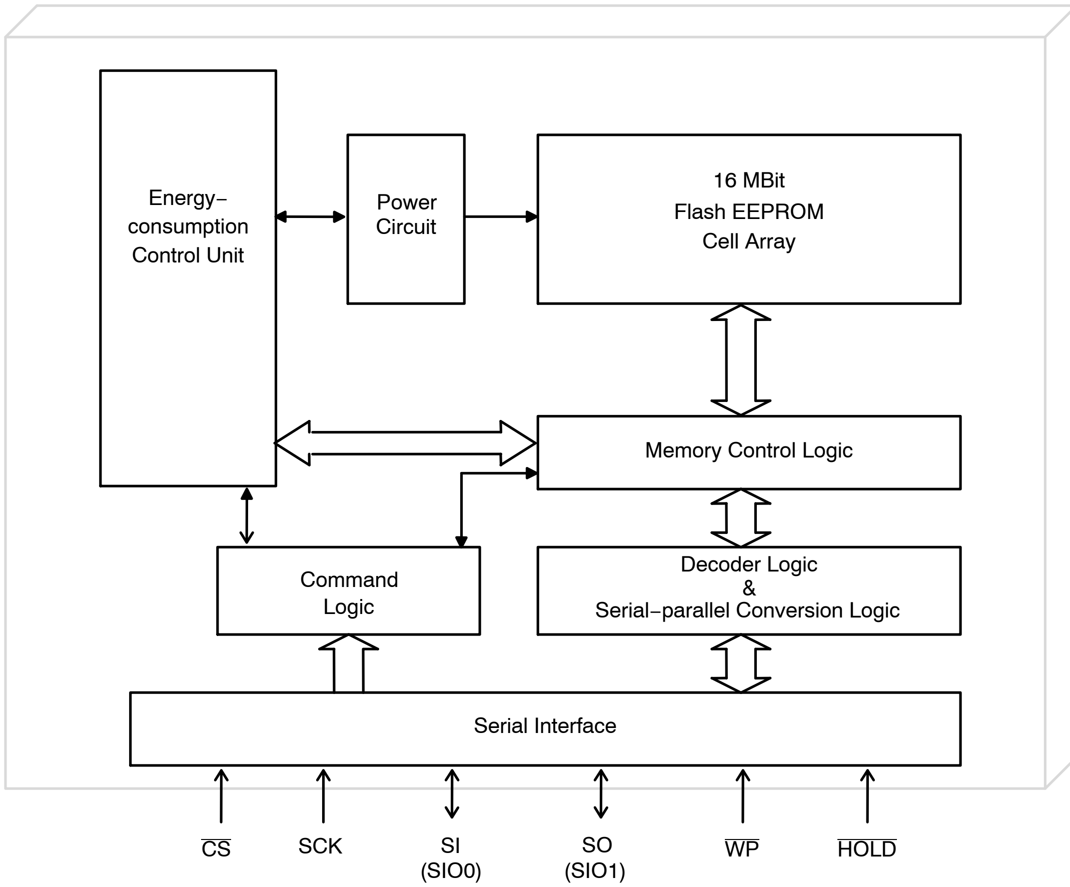


Figure 5. Block Diagram

DEVICE OPERATION

Standard SPI Modes

The read, erase, program and other required functions of the device are executed through the command registers. The serial I/O corrugate is shown in "*Figure 6. SPI Modes*" and the command list are shown in "*Table 5. Command Settings (Standard SPI)*". At the falling $\overline{CS}$ edge the device is selected, and serial input is enabled for the commands, addresses, etc. These inputs are normalized in 8 bit units and taken into the device interior in synchronization with the rising edge of SCK, which causes the device to execute operation according to the command that is input.

The LE25S161 supports both serial interface SPI mode 0 and SPI mode 3. At the falling $\overline{CS}$ edge, SPI mode 0 is automatically selected if the logic level of SCK is low, and SPI mode 3 is automatically selected if the logic level of SCK is high.

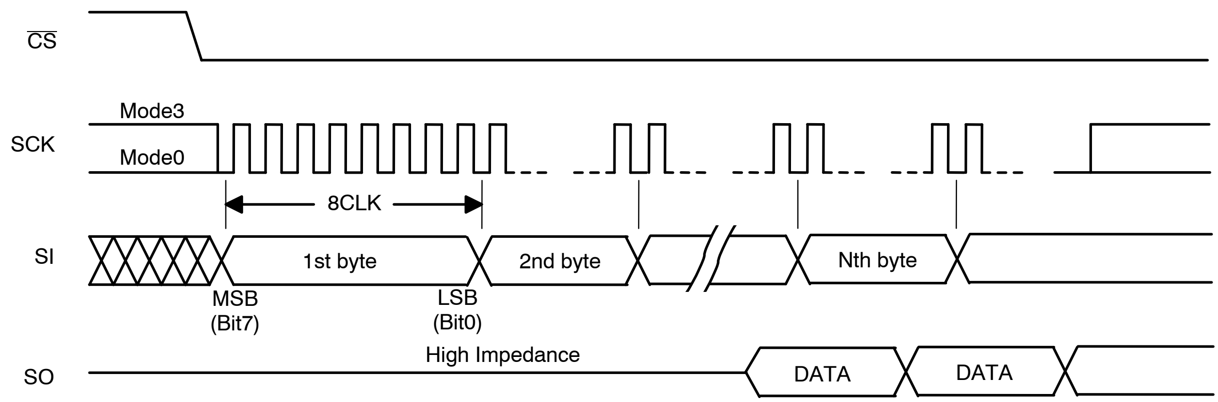


Figure 6. SPI Modes

Dual SPI Modes

The LE25S161 supports Dual SPI operations when using "Dual Output Read (RDDO: 3Bh)", "Dual I/O Read (RDIO: BBh)". The SI and SO pins change into the input/output pin (SIOx) during the Dual SPI modes. The command list is shown in "*Table 6. Command Settings (Dual SPI)*".

Table 4. PIN CONFIGURATIONS AT DUAL SPI MODE

Standard SPI		Dual SPI
SI	→	SIO0
SO	→	SIO1

Table 5. COMMAND SETTINGS (STANDARD SPI) – MAX: 70 MHz (EXCEPT RDLP)

Command	Description (Clock Number)	1st Byte (0–7)	2nd Byte (8–15)	3rd Byte (16–23)	4th Byte (24–31)	5th Byte (32–39)	6th Byte (40–47)	Nth Byte (8N–8 to 8N–1)
WREN	Write Enable	06h						
WRDI	Write Disable	04h						
RDSR	Read Status Register	05h						
WRSR	Write Status Register	01h	DATA					
RDLP	Low–Power Read (Max: 33.33 MHz)	03h	A23–A16	A15–A8	A7–A0	RD (Note 5)	RD (Note 5)	RD (Note 5)
RDHS	High–Speed Read	0Bh	A23–A16	A15–A8	A7–A0	X	RD (Note 5)	RD (Note 5)
SSE	Small Sector Erase (4 kB)	20h / D7h	A23–A16	A15–A8	A7–A0			
SE	Sector Erase (64 kB)	D8h	A23–A16	A15–A8	A7–A0			
CHE	Chip Erase (16 Mbits)	60h / C7h						
PP	Normal Page Program	02h	A23–A16	A15–A8	A7–A0	PD (Note 6)	PD (Note 6)	PD (Note 6)
PPL	Low–Power Page Program	0Ah						
WSUS	Write Suspend	B0h						
RESM	Resume	30h						
RJID	Read JEDEC ID	9Fh	Manufacture (62h)	Memory Type (16h)	Capacity (15h)			
RID	Read Device ID (Exit power down mode)	ABh	X	X	X	Device ID (88h)		
RSFDP	Read SFDP	5Ah	A23–A16	A15–A8	A7–A0	X	RD (Note 5)	RD (Note 5)
DP	Deep Power Down	B9h						
EDP	Exit Deep Power Down	ABh						
RSTEN	Reset Enable	66h						
RST	Reset	99h						

1. “X” signifies “don’t care” (that is to say, any value may be input).
2. “Z” signifies “high–impedance”.
3. The “h” following each code indicates that the number given is in hexadecimal notation.
4. Addresses A23 to A21 for all commands are “Don’t care”.
5. “RD” Read data on SO.
6. “PD” Page Program data on SO.

Table 6. COMMAND SETTINGS (DUAL SPI) – MAX: 50 MHz

Command	Description (Clock Number)	1st Byte (0–7)	2nd Byte (8–15)	3rd Byte (16–23)	4th Byte (24–31)	5th Byte (32–39)	6th Byte (40–47)	Nth Byte (8N–8 to 8N–1)
RDDO	Dual Output Read	3Bh	A23–A16	A15–A8	A7–A0	Z	RDD (Note 11)	RDD (Note 11)
RDIO	Dual I/O Read	BBh	A23–A8 (Note 12)	A7–A0 (Note 12), X, Z	RDD (Note 11)	RDD (Note 11)	RDD (Note 11)	RDD (Note 11)

7. “X” signifies “don’t care” (that is to say, any value may be input).
8. “Z” signifies “high–impedance”.
9. The “h” following each code indicates that the number given is in hexadecimal notation.
10. Addresses A23 to A21 for all commands are “Don’t care”.
11. “RDD” Dual Read data:
    SIO0 = (Bit6, Bit4, Bit2, Bit0)
    SIO1 = (Bit7, Bit5, Bit3, Bit1)
12. Dual SPI address input from SIO0 and SIO1:
    SIO0 = (A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0)
    SIO1 = (A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1)

MEMORY ORGANIZATION

Table 7. MEMORY ORGANIZATION (16 Mbits)

Sector (64 kB) Symbol: SE	Small Sector (4 kB) Symbol: SSE	Address Space (A23 to A0)	
31	SSE[511]	1FF000h	1FFFFFh
	to		
	SSE[496]	1F0000h	1F0FFFh
30 to 6	SSE[495]	1EF000h	1EFFFFh
	to		
	SSE[96]	060000h	060FFFh
5	SSE[95]	05F000h	05FFFFh
	to		
	SSE[80]	050000h	050FFFh
4	SSE[79]	04F000h	04FFFFh
	to		
	SSE[64]	040000h	040FFFh
3	SSE[63]	03F000h	03FFFFh
	to		
	SSE[48]	030000h	030FFFh
2	SSE[47]	02F000h	02FFFFh
	to		
	SSE[32]	020000h	020FFFh
1	SSE[31]	01F000h	01FFFFh
	to		
	SSE[16]	010000h	010FFFh
0	SSE[15]	00F000h	00FFFFh
	to		
	SSE[4]	004000h	004FFFh
	SSE[3]	003800h	003FFFh
		003000h	0037FFh
	SSE[2]	002800h	002FFFh
		002000h	0027FFh
	SSE[1]	001800h	001FFFh
		001000h	0017FFh
	SSE[0]	000800h	000FFFh
		000000h	0007FFh

STATUS REGISTERS

The status registers hold the operating and setting statuses inside the device, and this information can be read by Read Status Register (RDSR) and the protect information can be rewritten by Write Status Register (WRSR). There are 8 bits in total, and "*Table 8. Status registers*" gives the significance of each bit.

Table 8. STATUS REGISTERS

Bit	Name	Logic	Function	Power−on Time Information
Bit0	$\overline{\text{RDY}}$	0	Ready	3
		1	Erase/Program	
Bit1	WEN	0	Write disabled	0
		1	Write enabled	
Bit2	BP0	0	Block protect information Protected area switch	Nonvolatile information
		1		
Bit3	BP1	0		
		1		
Bit4	BP2	0		
		1		
Bit5	TB	0	Block protect Upper side/Lower side switch	Nonvolatile information
		1		
Bit6	SUS	0	Erase/Program is not suspended	0
		1	Erase/Program suspended	
Bit7	SRWP	0	Write Status Register enabled	Nonvolatile information
		1	Write Status Register disabled	

13. All non−volatile bits of the status registers−1 are set "0" in the factory.

Contents of Each Status Register

$\overline{\text{RDY}}$ (Bit 0)

The $\overline{\text{RDY}}$ register is for detecting the write (Program, Erase and Write Status Register) end. When it is "1", the device is in a busy state, and when it is "0", it means that write is completed.

WEN (Bit 1)

The WEN register is for detecting whether the device can perform write operations. If it is set to "0", the device will not perform the write operation even if the write command is input. If it is set to "1", the device can perform write operations in any area that is not block−protected.

WEN can be controlled using the write enable (WREN) and write disable (WRDI). By inputting the write enable (WREN: 06h), WEN can be set to "1" by inputting the write disable (WRDI: 04h), it can be set to "0." In the following states, WEN is automatically set to "0" in order to protect against unintentional writing.

- At power−on
- Upon completion of Erase (SSE, SE, or CHE)
- Upon completion of Page Program (PP or PPL)
- Upon completion of Write Status Register (WRSR)

*If a write operation has not been performed inside the LE25S161 because, for instance, the command input for any of the write operations (SSE, SE, CHE, PP, PPL or WRSR) has failed or a write operation has been performed for a protected address, WEN will retain the status established prior to the issue of the command concerned. Furthermore, its state will not be changed by a read operation.

BP0, BP1, BP2, TB (Bits 2, 3, 4, 5)

Block Protect: BP0, BP1, BP2 and TB are status register bits that can be rewritten, and the memory space to be protected can be set depending on these bits. For the setting conditions, refer to "*Table 9. Protected Level Setting Conditions*".

BP0, BP1, and BP2 are used to select the protected area and TB to allocate the protected area to the higher−order address area or lower−order address area.

Table 9. PROTECTION LEVEL SETTING CONDITIONS

Protected Level	Protected Block	Status Register Bits				Protected Area
		TB	BP2	BP1	BP0	
0	Whole area unprotected	X	0	0	0	None
T1	Upper side 1/32 protected	0	0	0	1	1F0000h to 1FFFFFh
T2	Upper side 1/16 protected	0	0	1	0	1E0000h to 1FFFFFh
T3	Upper side 1/8 protected	0	0	1	1	1C0000h to 1FFFFFh
T4	Upper side 1/4 protected	0	1	0	0	180000h to 1FFFFFh
T5	Upper side 1/2 protected	0	1	0	1	100000h to 1FFFFFh
B1	Lower side 1/32 protected	1	0	0	1	000000h to 00FFFFh
B2	Lower side 1/16 protected	1	0	1	0	000000h to 01FFFFh
B3	Lower side 1/8 protected	1	0	1	1	000000h to 03FFFFh
B4	Lower side 1/4 protected	1	1	0	0	000000h to 07FFFFh
B5	Lower side 1/2 protected	1	1	0	1	000000h to 0FFFFFh
6	Whole area protected	X	1	1	X	000000h to 1FFFFFh

14. Chip Erase is enabled only when the protection level is 0.

SUS (Bit 6)

The SUS register indicates when Erase/Program operation has been suspended. The SUS becomes “1” when the Erase/Program operation has been suspended (WSUS: B0h). The SUS is cleared to “0” by Resume (RESM: 30h) or re−erase/program (SSE, SE, CHE, PP, PPL).

SRWP (Bit 7)

Write Status Register protect SRWP is the bit for protecting the status registers, and its information can be rewritten. When SRWP is “1” and the logic level of the $\overline{\text{WP}}$ pin is low, the Write Status Register (WRSR: 01h) is ignored, and status registers BP0, BP1, BP2, TB and SRWP are protected. When the logic level of the $\overline{\text{WP}}$ pin is high, the status registers are not protected regardless of the SRWP state. The SRWP setting conditions are shown in “Table 10. SRWP Setting Conditions”.

Table 10. SRWP SETTING CONDITIONS

$\overline{\text{WP}}$ Pin	SRWP	Status Register Protect State
0	0	Unprotected
	1	Protected
1	0	Unprotected
	1	Unprotected

DESCRIPTION OF COMMANDS AND OPERATIONS

A detailed description of the functions and operations corresponding to each command is presented below.

Read Status Register (RDSR)

The contents of the status registers can be read using the Read Status Register (RDSR). This command can be executed even during the following operations.

- Erase (SSE, SE or CHE)
- Page Program (PP or PPL)
- Write Status Register (WRSR)

"*Figure 7. Read Status Register (RDSR)*" shows the timing waveforms.

The sequence of RDSR operation:

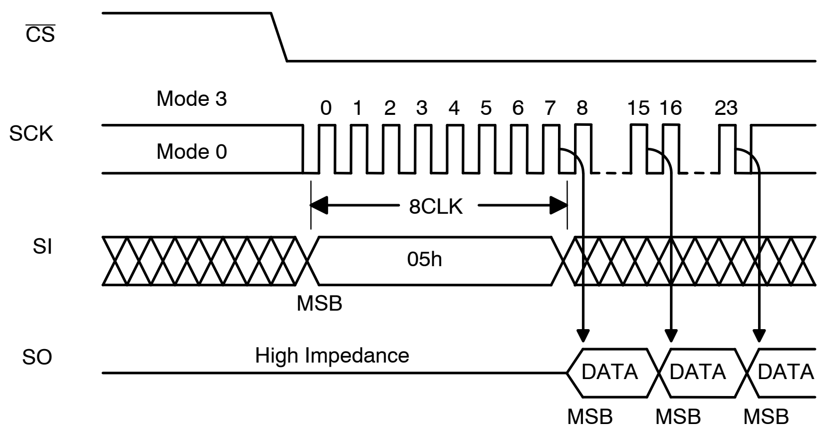
$\overline{CS}$ goes to low → input RDSR command (05h) → Status Register data (SRWP, SUS, TB, BP2, BP1, BP0,WEN, $\overline{RDY}$) out on SO →→

→ completed by $\overline{CS}$ = high

*The data output starts from the falling edge of SCK (7th clock)

This command outputs the contents of the status registers synchronized to the falling edge of the clock (SCK).

If the clock input is continued after bit0 ($\overline{RDY}$) has been output, the data is output by returning to bit7 (SRWP) that was first output, after which the output is repeated for as long as the clock input is continued. The data can be read by this command at any time (even during a program, erase cycle). By setting $\overline{CS}$ to high, the device is deselected, and Read JEDEC ID cycle is completed. While the device is deselected, the output pin SO is in a high−impedance state



- DATA: Status Resister, "*Table 8. Status Register*"

Figure 7. Read Status Register (RDSR)

Write Status Register (WRSR)

The information in status registers BP0, BP1, BP2, TB and SRWP can be rewritten using this command. bit0 ($\overline{\text{RDY}}$), bit1 (WEN) and bit6 (SUS) are read−only bits and cannot be rewritten. The information in bits BP0, BP1, BP2, TB and SRWP is stored in the non−volatile memory, and when it is written in these bits, the contents are retained even at power−down.

"*Figure 8. Write Status Register (WRSR)*" shows the timing waveforms.

"*Figure 37. Write Status Register Flowcharts*" shows the flowcharts.

The sequence of WRSR operation:

$\overline{\text{CS}}$ goes to low → input WRSR command (01h)

→ Status Register data input on SI

→ $\overline{\text{CS}}$ goes to high (be executed by the rising $\overline{\text{CS}}$ edge)

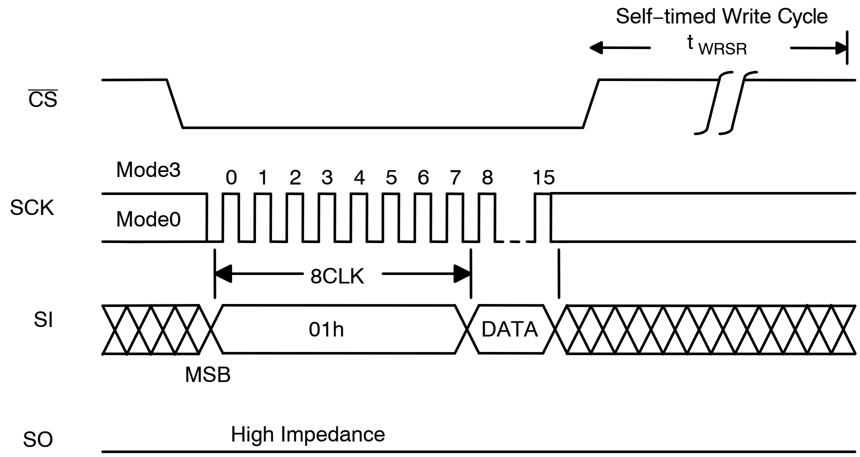


Figure 8. Write Status Register (WRSR)

Write Enable (WREN)

Before performing any of the operations listed below, the device must be placed in the write enable state.

- Erase (SSE, SE, CHE or CHE)
- Page Program (PP or PPL)
- Write Status Register (WRSR)

Operation is the same as for setting status register WEN to "1", and the state is enabled by this command.

"*Figure 9. Write Enable (WREN)*" shows the timing waveforms.

The sequence of WREN operation:

$\overline{\text{CS}}$ goes to low → input WREN command (06h)

→ $\overline{\text{CS}}$ goes to high (be executed by the rising $\overline{\text{CS}}$ edge)

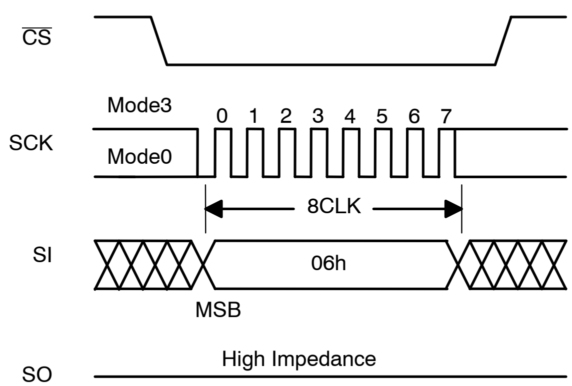


Figure 9. Write Enable (WREN)

Write Disable (WRDI)

This command sets status register WEN to "0" to prohibit unintentional writing. The write disable state (WEN "0") is exited by setting WEN to "1" using the write enable (WREN: 06h).

"*Figure 10. Write Disable (WRDI)*" shows the timing waveforms.

The sequence of WRDI operation:

$\overline{\text{CS}}$ goes to low → input WRDI command (04h)

→ $\overline{\text{CS}}$ goes to high (be executed by the rising $\overline{\text{CS}}$ edge)

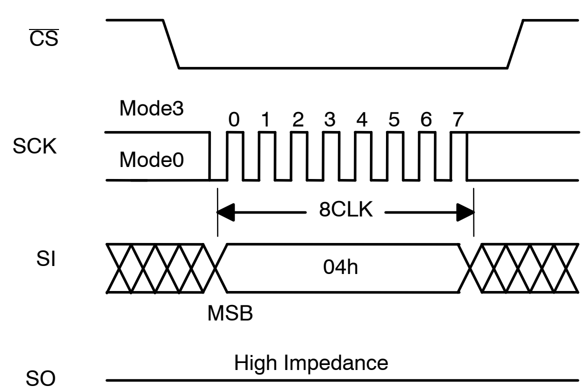


Figure 10. Write Disable (WRDI)

Standard SPI Read

There are two Read commands, "Low−Power Read (RDLP: 03h)" and "High−Speed Read (RDHS: 0Bh)".

Low−Power Read command (RDLP) − Maximum Clock Frequency: 33.33 MHz

This command is for reading data out.

"*Figure 11. Low−Power Read (RDLP)*" shows the timing waveforms.

The sequence of RDLP operation:

$\overline{CS}$ goes to low → input RDLP command (03h) → 3 Byte address (A23 − A0) input on SI

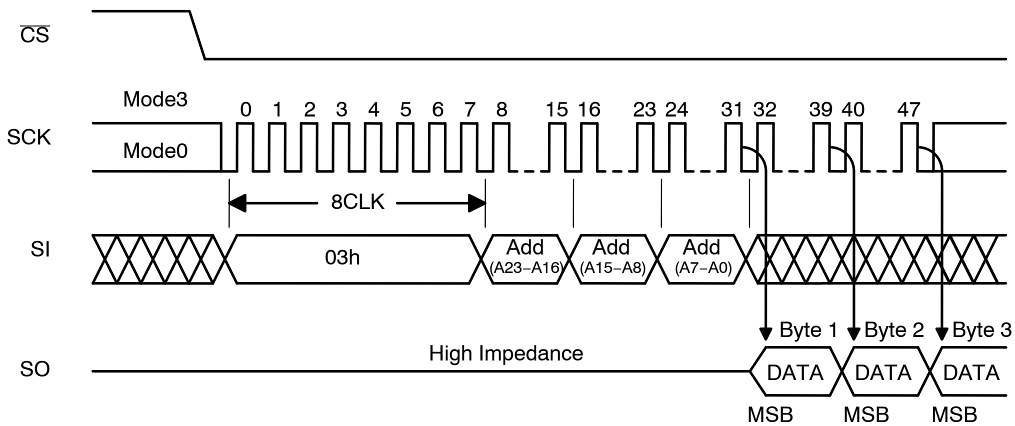
→ the corresponding data out on SO

→ continuous data out (n−byte) →→

→ completed by $\overline{CS}$ = high

*The data output starts from the falling edge of SCK (31th clock)

The Address is latched on rising edge of SCK, and the corresponding data is shifted out on SO by the falling edge of SCK. The address is automatically incremented to the next higher address after each byte data is shifted out. If the SCK input is continued after the internal address arrives at the highest address (1FFFFFh), the internal address returns to the lowest address (000000h). By setting $\overline{CS}$ to high, the device is deselected, and the read cycle is completed. While the device is deselected, the output pin SO is in a high−impedance state.



• Address A23 to A21 are "Don't care".

Figure 11. Low−Power Read (RDLP)

High−Speed Read Command (RDHS) − Maximum Clock frequency: 70 MHz

This command is for reading data out at the high frequency operation.

"*Figure 12. High−Speed Read (RDHS)*" shows the timing waveforms.

The sequence of RDHS operation:

$\overline{CS}$ goes to low → input RDHS command (0Bh) → 3 Byte address (A23 − A0) input on SI

→ 1 byte dummy cycle → the corresponding data out on SO

→ continuous data out (n−byte) →→

→ completed by $\overline{CS}$ = high

*The data output starts from the falling edge of SCK(39th clock)

The Address is latched on rising edge of SCK. It is necessary to add 1 dummy byte cycle after address is latched, and the corresponding data is shifted out on SO by the falling edge of SCK. The address is automatically incremented to the next higher address after each byte data is shifted out. If the SCK input is continued after the internal address arrives at the highest address (1FFFFFh), the internal address returns to the lowest address (000000h). By setting $\overline{CS}$ to high, the device is deselected, and the read cycle is completed. While the device is deselected, the output pin SO is in a high−impedance state.

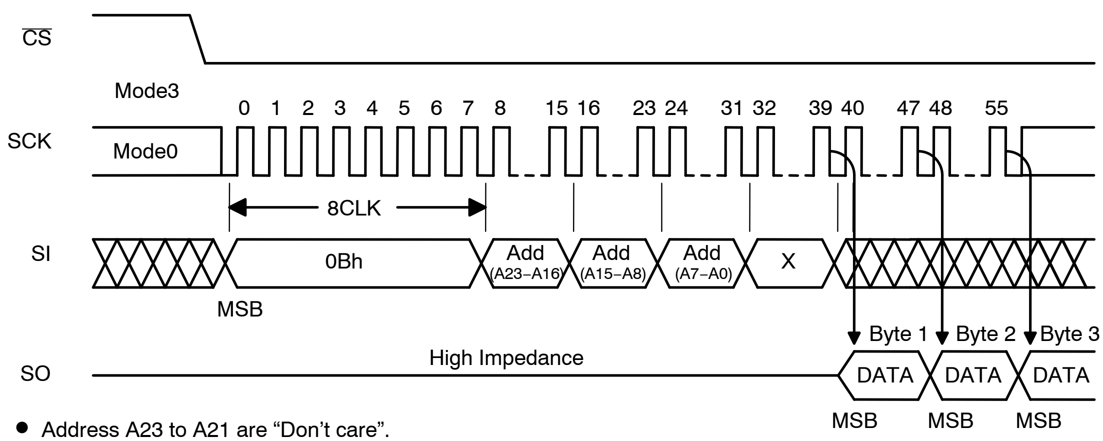


Figure 12. High−Speed Read (RDHS)

Dual Read

There are two Dual read commands, the Dual Output Read (RDDO) and the Dual I/O Read (RDIO).

They achieve the twice speed−up from "High−Speed Read (RDHS: 0Bh)". The command list is shown in "*Table 6. Command Settings (Dual SPI)*"

Table 11. PIN CONFIGURATIONS AT DUAL SPI MODE

Standard SPI		Dual SPI
SI	→	SIO0
SO	→	SIO1

Dual Output Read Command (RDDO) − Maximum Clock Frequency: 50 MHz

The SI and SO pins change into the input/output pin (SIOx) during this operation. It makes the data output x2 bit and has achieved a high−speed output. bit7, 5, 3 and bit1are output from SIO0. bit6, 4, 2 and bit0 are output from SIO1.

"*Figure 13. Dual Output Read (RDDO)*" shows the timing waveforms.

The sequence of RDDO operation:

$\overline{CS}$ goes to low → input RDDO command (3Bh) → 3 Byte address (A23 − A0) input on SI

→ 1 byte dummy cycle → the corresponding data out on SI/SIO0 and SO/SIO1

→ continuous data out (n−byte) per 4 clock →→

→ completed by $\overline{CS}$ = high

*The data output starts from the falling edge of SCK (39th clock)

	Output Data
SI/SIO0	bit6, 4, 2, 0
SO/SIO1	bit7, 5, 3, 1

The Address is latched on rising edge of SCK. It is necessary to add 1 dummy byte cycle after address is latched, and the corresponding data is shifted out on SI/SIO0 and SO/SIO1 by the falling edge of SCK. The address is automatically incremented to the next higher address after each byte data (4 clock cycles) is shifted out. If the SCK input is continued after the internal address arrives at the highest address (1FFFFFh), the internal address returns to the lowest address (000000h). By setting $\overline{CS}$ to high, the device is deselected, and the read cycle is completed. While the device is deselected, the output pin SO is in a high−impedance state.

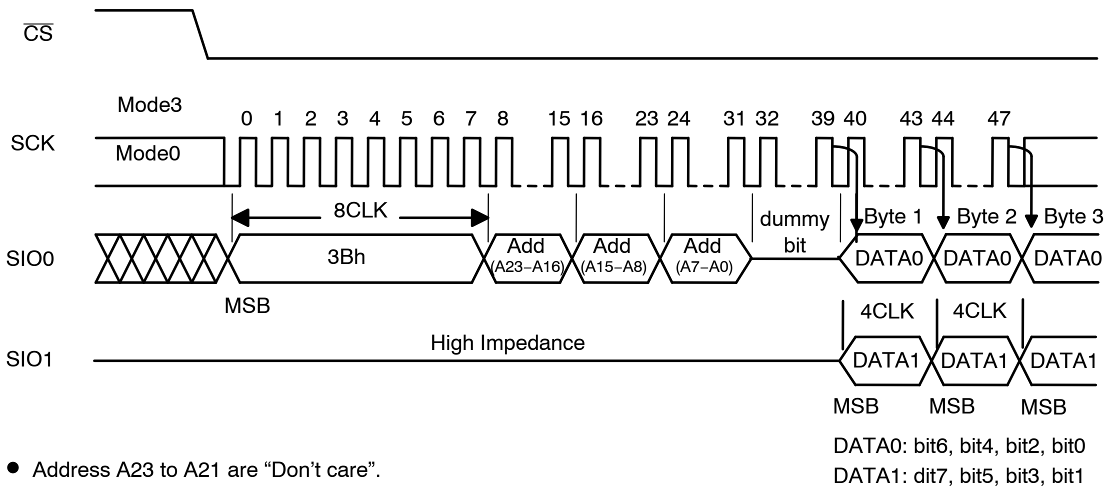


Figure 13. Dual Output Read (RDDO)

Dual I/O Read Command (RDIO) – Maximum Clock Frequency: 50 MHz

The SI and SO pins change into the input/output pin (SIOx) during this operation. It makes the address input and data output x2 bit and has achieved a high−speed output. Add1 (A23, A21, –, A3 and A1) is input from SIO1 and Add0 (A22, A20, –, A2 and A0) is input from SIO0. bit7, 5, 3 and bit1 are output from SIO0. bit6, 4, 2 and bit0 are output from SIO1.

“*Figure 14. Dual I/O Read (RDIO)*” shows the timing waveforms.

The sequence of RDIO operation:

$\overline{\text{CS}}$ goes to low → input RDIO command (BBh)

→ 3 Byte address (A23 – A0) input on SI/SIO0 and SO/SIO1 by 12 clock cycle

→ 2 dummy clock (SI/SIO0 and SO/SIO1 are don’t care)

+ 2 dummy clock (must set SI/SIO0 and SO/SIO1 high impedance)

→ the corresponding data out on SI/SIO0 and SO/SIO

→ continuous data out (n−byte) per 4 clock →→

→ completed by $\overline{\text{CS}}$ = high

*The data output starts from the falling edge of SCK (23th clock)

	Input Address	Output Data
SI/SIO0	A22, 20, 18 –, A2, A0	bit6, 4, 2, 0
SO/SIO1	A23, 21, 19 –, A3, A1	bit7, 5, 3, 1

The Address is latched on rising edge of SCK. It is necessary to add 4 dummy clocks after address is latched, 2CLK of the latter half of the dummy clock is in the state of high impedance, the controller can switch I/O for this period. The corresponding data is shifted out on SI/SIO0 and SO/SIO1 by the falling edge of SCK. The address is automatically incremented to the next higher address after each byte data (4 clock cycles) is shifted out. If the SCK input is continued after the internal address arrives at the highest address (1FFFFFh), the internal address returns to the lowest address (000000h). By setting $\overline{\text{CS}}$ to high, the device is deselected, and the read cycle is completed. While the device is deselected, the output pin SO is in a high−impedance state.

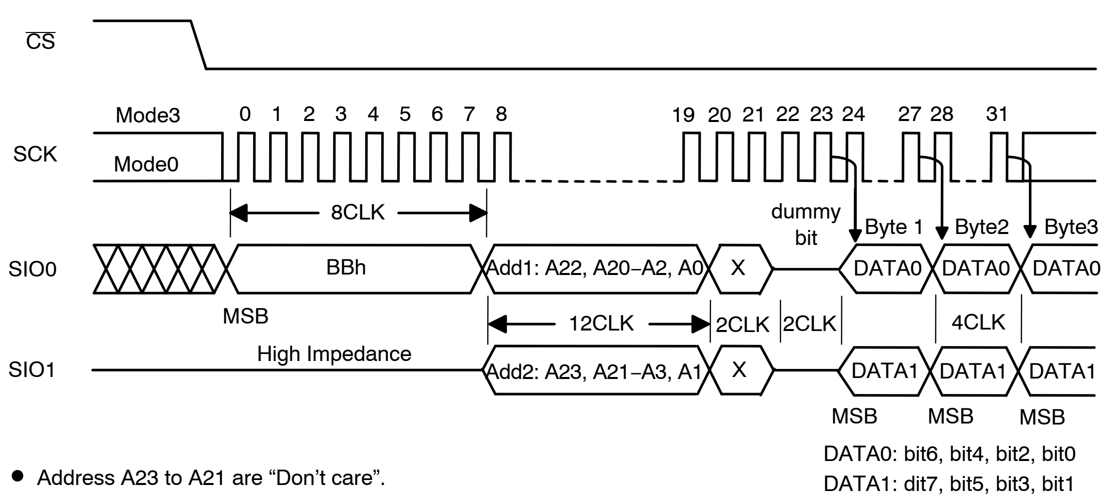


Figure 14. Dual I/O Read (RDIO)

Small Sector Erase (SSE)

Small Sector Erase is an operation that sets the memory cell data in any small sector to “1”. A small sector consists of 4 kbytes.

“*Figure 15. Small Sector Erase (SSE)*” shows the timing waveforms.

“*Figure 38. Small Sector Erase Flowcharts*” shows the flowcharts.

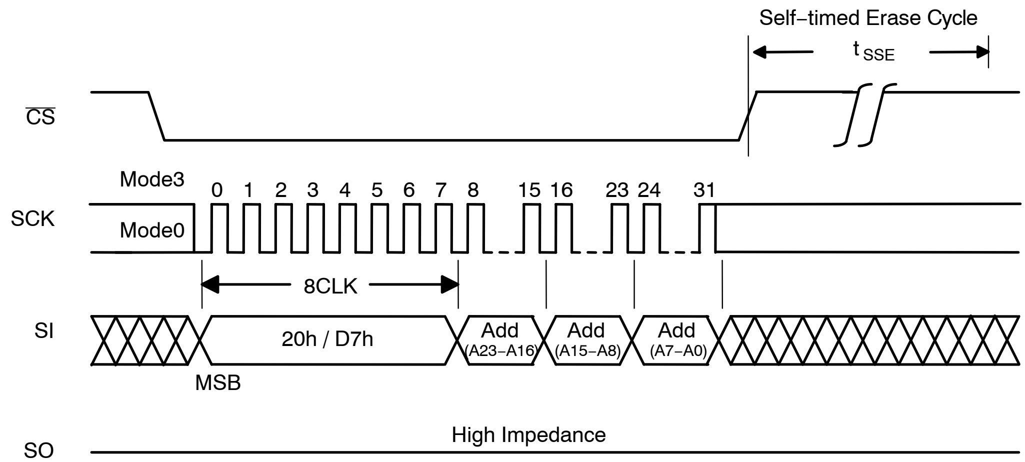
The sequence of SSE operation:

$\overline{CS}$ goes to low → input SSE command (20h or D7h) → 3 Byte address (A23 − A0) input on SI

→ $\overline{CS}$ goes to high (be executed by the rising $\overline{CS}$ edge)

*A20 to A12 are valid address

After the correct input sequence the internal erase operation is executed by the rising $\overline{CS}$ edge, and it is completed automatically by the control exercised by the internal timer (tSSE). The end of erase operation can also be detected by status register ($\overline{RDY}$).



- Address A23 to A21, A11 to A0 are “Don’t care”.

Figure 15. Small Sector Erase (SSE)

Sector Erase (SE)

Sector Erase is an operation that sets the memory cell data in any sector to “1”. A sector consists of 64 kbytes.

“*Figure 16. Sector Erase (SE)*” shows the timing waveforms.

“*Figure 39. Sector Erase Flowcharts*” shows the flowcharts.

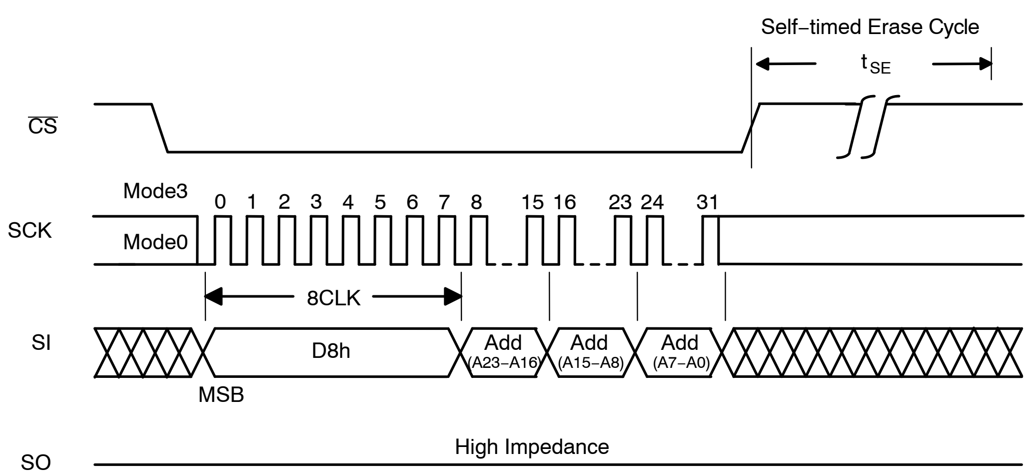
The sequence of SE operation:

$\overline{CS}$ goes to low → input SE command (D8h) → 3 Byte address (A23 − A0) input on SI

→ $\overline{CS}$ goes to high (be executed by the rising $\overline{CS}$ edge)

*A20 to A16 are valid address

After the correct input sequence the internal erase operation is executed by the rising $\overline{CS}$ edge, and it is completed automatically by the control exercised by the internal timer (tSE). The end of erase operation can also be detected by status register ($\overline{RDY}$).



- Address A23 to A21, A15 to A0 are “Don’t care”.

Figure 16. Sector Erase (SE)

Chip Erase (CHE)

Chip Erase is an operation that sets the memory cell data in all sectors to “1”.

“*Figure 17. Chip Erase (CHE)*” shows the timing waveforms.

“*Figure 40. Chip Erase Flowcharts*” shows the flowcharts

The sequence of CHE operation:

$\overline{CS}$ goes to low → input CHE command (60h or C7h)

→ $\overline{CS}$ goes to high (be executed by the rising $\overline{CS}$ edge)

After the correct input sequence the internal erase operation is executed by the rising $\overline{CS}$ edge, and it is completed automatically by the control exercised by the internal timer (tSE). The end of erase operation can also be detected by status register ($\overline{RDY}$).

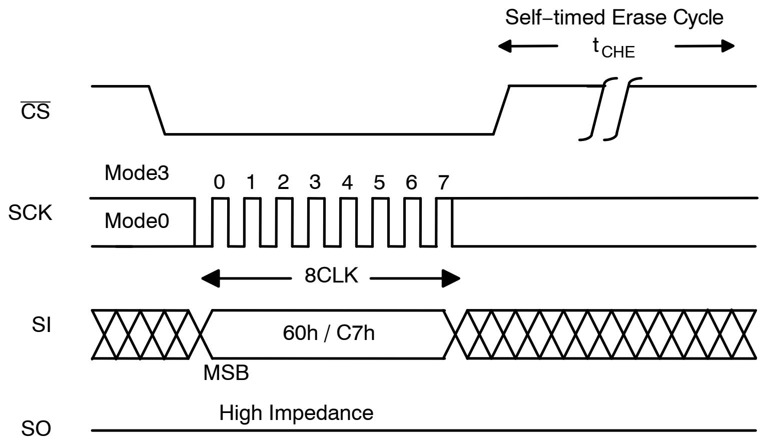


Figure 17. Chip Erase (CHE)

Page Program

Normal Page Program (PP)

Low−Power Page Program (PPL)

There are two Page Program commands, Normal program (PP: 02h) and Low−Power program (PPL: 0Ah). These two commands are completely functionally the same. By selecting the Low−Power program (PPL), the operating current is reduced, but the program cycle time is extended. (Iccpp > Iccppl, tPPL > tPP)

Page Program is an operation that programs any number of bytes from 1 to 256 bytes within the same sector page (page addresses: A20 to A8). Before initiating Page Program, the data on the page concerned must be erased using Small Sector Erase, Sector Erase, or Chip Erase. Page Program (PP, PPL) allows only previous erased data (FFh).

“*Figure 18. Normal Page Program (PP)*”. “*Figure 19. Low−power Page Program (PPL)*” shows the timing waveforms.

“*Figure 41. Page Program Flowcharts*” shows the flowcharts.

The sequence of PP or PPL operation:

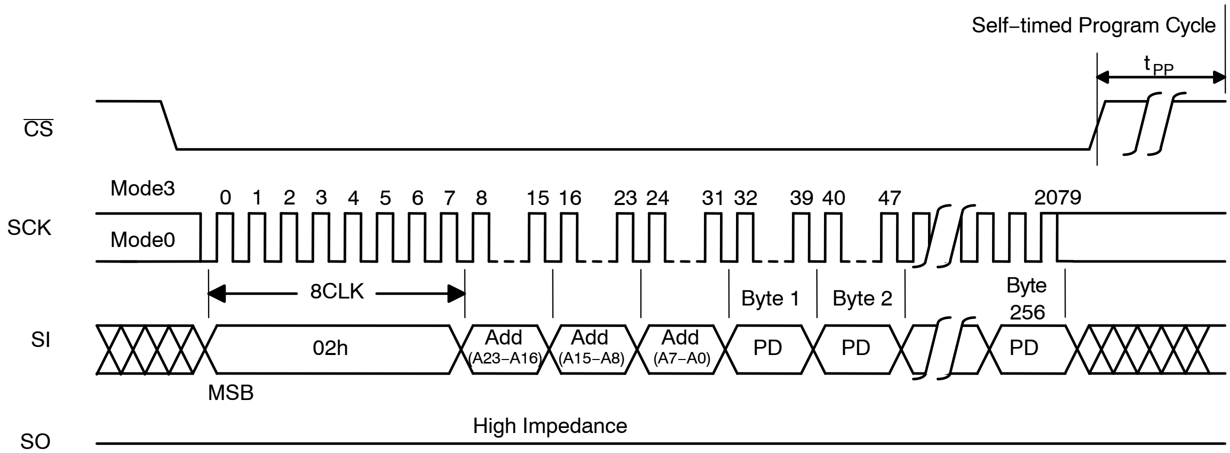
$\overline{CS}$ goes to low → input PP command (02h) or PPL command (0Ah)

→ 3 Byte address (A23 − A0) input on SI

→ n−Byte data input on SI →→

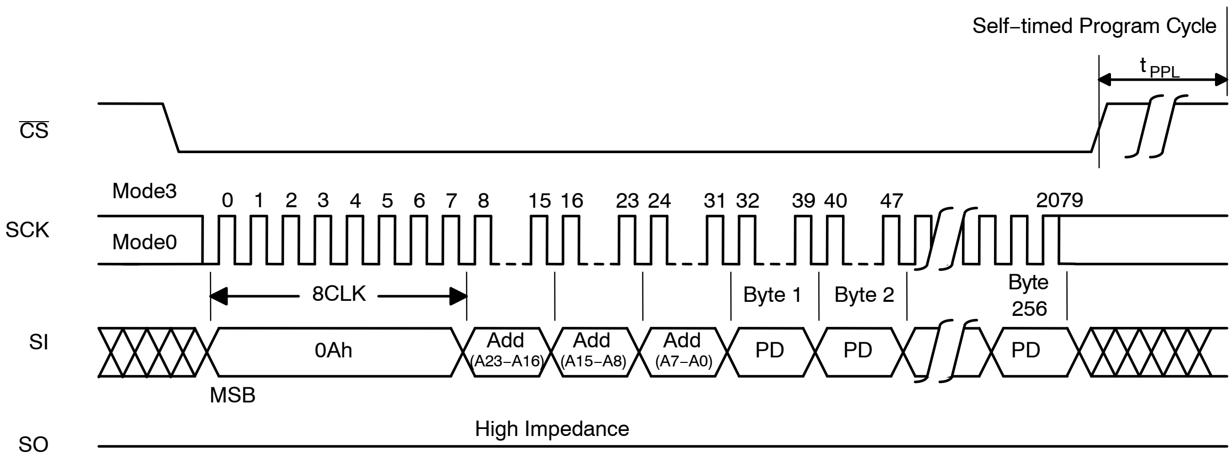
→ $\overline{CS}$ goes to high (be executed by the rising $\overline{CS}$ edge)

The program data must be loaded in 1−byte increments. If the data loaded has exceeded 256 bytes, the 256 bytes loaded last are programmed. After the correct input sequence the internal program operation is executed by the rising $\overline{CS}$ edge, and it is completed automatically by the control exercised by the internal timer (tPP or tPPL). The end of program operation can also be detected by status register ($\overline{RDY}$).



- Address A23 to A21, A15 to A0 are "Don't care".

Figure 18. Normal Page Program (PP)



- Address A23 to A21, A15 to A0 are "Don't care".

Figure 19. Low–Power Page Program (PPL)

Write Suspend (WSUS)

The Write Suspend (WSUS) allow the system to interrupt Small Sector Erase (SSE), Sector Erase (SE), Chip Erase (CHE) or Page Program (PP, PPL).

"*Figure 20. Write Suspend (WSUS)*" shows the timing waveforms.

The sequence of WSUS operation:

$\overline{\text{CS}}$ goes to low → input WSUS command (B0h)

→ $\overline{\text{CS}}$ goes to high (be executed by the rising $\overline{\text{CS}}$ edge)

After the command has been input, the device becomes consumption current equivalent to standby within 20 μs. The recovery time (tRSUS) is needed before next command from suspend. The internal operation status could be checked by using status register $\overline{\text{RDY}}$ bit or SUS bit, but the device will not accept another command until it is ready.

- The Write Suspend is valid Erase cycle (SSE, SE and CHE) or Program cycle (PP, PPL).
- If the Erase (SSE, SE, CHE) or Program (PP, PPL) entry during the suspension, the suspension will be canceled automatically. And a new Erase (SSE, SE, CHE), Program (PP, PPL) will be executed. In this case, it is necessary to erase/program the suspended area again.
- During Write Suspend, Read (RDSR, RDLP, RDHS, RDDO, RDIO) and Resume (RESM) can be accepted.
- If the Software Reset is executed during the suspension, the suspension will be canceled automatically.

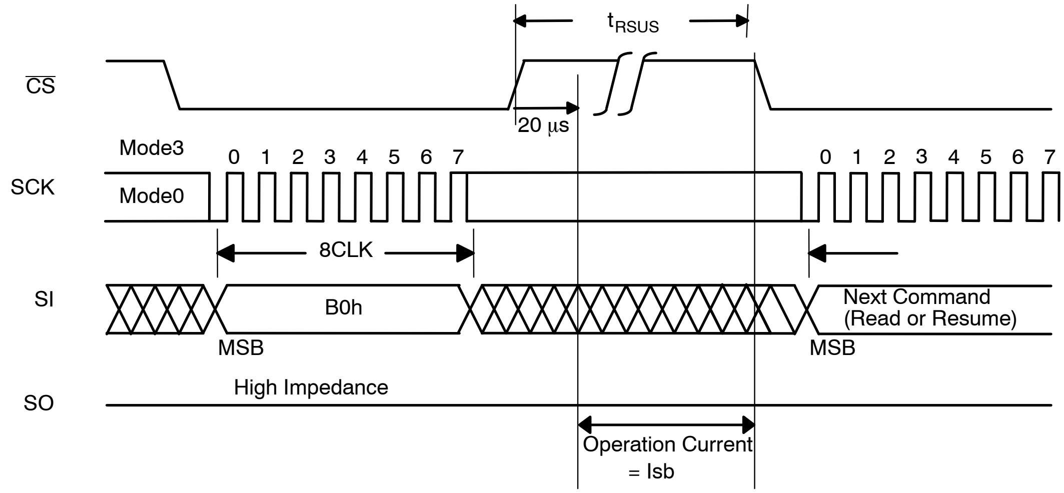


Figure 20. Write Suspend (WSUS)

Resume (RESM)

This command (RESM) restarts erase cycle (SSE, SE, CHE) or program cycle (PP, PPL) that was suspended.

"*Figure 21. Resume (RESM)*" shows the timing waveforms.

The sequence of RESM operation:

$\overline{CS}$ goes to low → input RESM command (30h)
→ $\overline{CS}$ goes to high (be executed by the rising $\overline{CS}$ edge)

The internal operation status could be checked by using status register $\overline{RDY}$ bit or SUS bit.

This command will be ignored if the previous Write Suspend operation was interrupted by unexpected power off or re−erase/program (cancel of suspend) or Software Reset (RST). To execute Write Suspend (WSUS) again after Resume, it is necessary to wait for some time (tSUS).

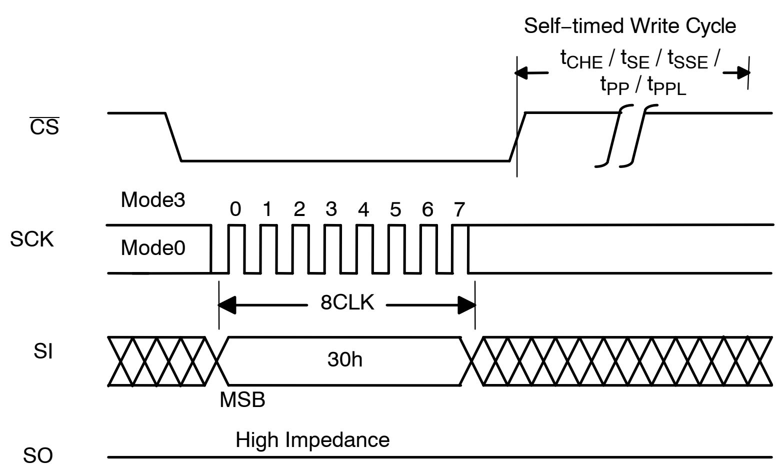


Figure 21. Resume (RESM)

Read ID

Read ID is an operation that reads the manufacturer code (RJID) and device ID information (RID). These Read ID commands are not accepted during writing. There are two methods of reading the silicon ID, each of which is assigned a device ID.

Read JEDEC ID (RJID)

This command (RJID) is compatible with the JEDEC standard for SPI compatible serial memories.

"*Table 12. JEDEC ID codes*" lists the silicon ID codes.

"*Figure 22. Read JEDEC ID (RJID)*" shows the timing waveforms.

The sequence of RJID operation:

$\overline{CS}$ goes to low → input RJID command (9Fh)

→ Manufacture code (62h) out on SO → Memory type code (16h) out on SO

→ Memory capacity code out on SO (15h) → Reserve code (00h) →→

→ completed by $\overline{CS}$ = high

*The 4−byte code is output repeatedly as long as clock inputs are present
*The data output starts from the falling edge of SCK (7th clock)

By setting $\overline{CS}$ to high, the device is deselected, and Read JEDEC ID cycle is completed. While the device is deselected, the output pin SO is in a high−impedance state.

Table 12. JEDEC ID CODES

		Output Code
Manufacturer code		62h
2 byte device ID	Memory type	16h
	Memory capacity code	15h (16 MBit)
Reserve code		00h

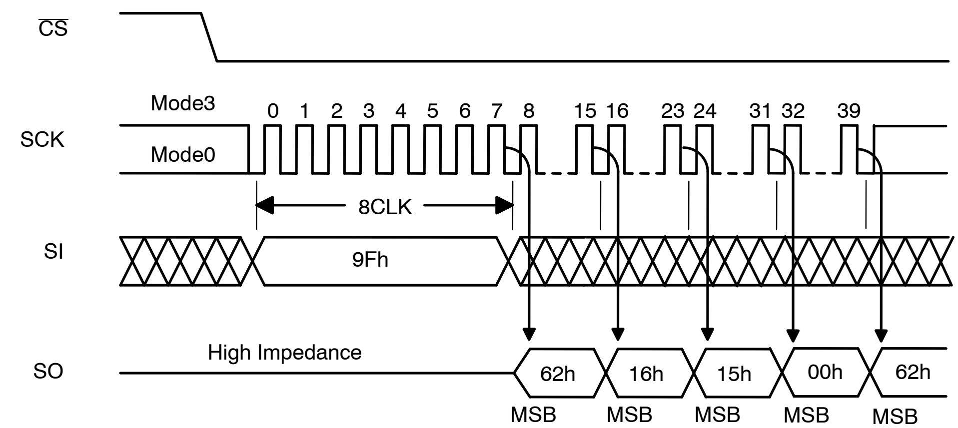


Figure 22. Read JEDEC ID (RJID)

Read Device ID (RID)

This command (RID) is an operation that reads the Device ID.

"*Table 13. Device ID Code*" lists the device ID codes.

"*Figure 23. Read Device ID (RID)*" shows the timing waveforms.

The sequence of RID operation:

$\overline{CS}$ goes to low → input RID command (ABh) → 3 byte dummy cycle

→ Device ID (88h) out on SO →→

→ completed by $\overline{CS}$ = high

*The Device ID (88h) is output repeatedly as long as clock inputs are present
*The data output starts from the falling edge of SCK (31th)

By setting $\overline{CS}$ to high, the device is deselected, and Read ID cycle is completed. While the device is deselected, the output pin SO is in a high−impedance state.

Table 13. DEVICE ID CODE

	Output Code
1 byte device ID	88h (LE25S161)

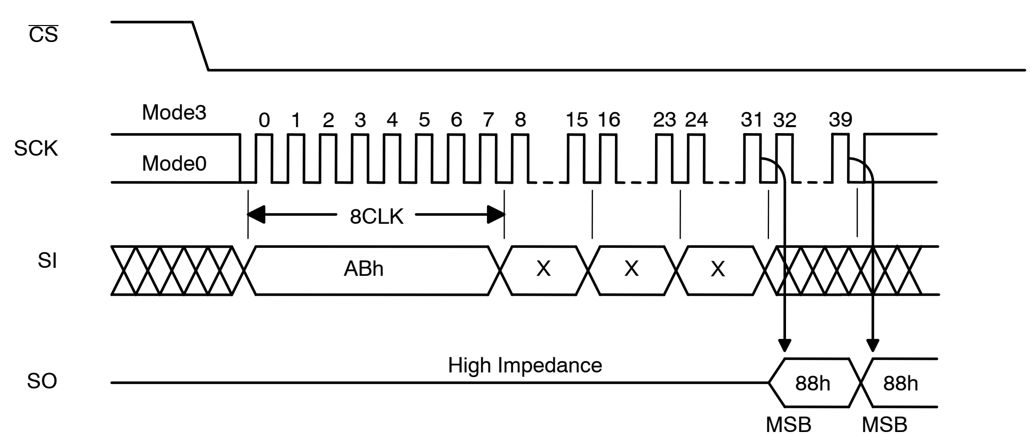


Figure 23. Read Device ID (RID)

Deep Power−down (DP)

The standby current can be further reduced with this command (DP).

"*Figure 24. Deep Power−down (DP)*" shows the timing waveforms.

The sequence of DP operation:

$\overline{CS}$ goes to low → input DP command (B9h)

→ $\overline{CS}$ goes to high (be executed by the rising $\overline{CS}$ edge)

The deep power−down command issued during an internal write operation will be ignored.

The deep power−down state is exited using the deep power−down exit (EDP). All other commands are ignored.

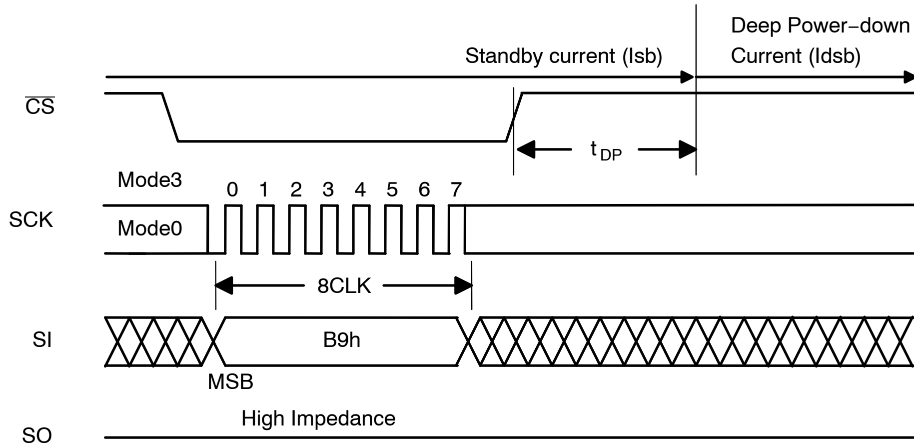


Figure 24. Deep Power−down (DP)

Exit Deep Power−down (EDP) / Read Device ID (RDDI)

The Exit Deep Power−down (EDP) / Read Device ID (RID) command is a multi−purpose command. It can be used to exit the device from the deep power−down state, or read the device ID information.

Exit Deep Power−down (EDP)

The exit deep power−down command consists only of the first byte cycle, and it is initiated by inputting (ABh).

"*Figure 25. Exiting from Deep Power−down*" shows the timing waveforms.

The sequence of EDP operation:

$\overline{CS}$ goes to low → input EDP command (ABh)

→ $\overline{CS}$ goes to high (be executed by the rising $\overline{CS}$ edge)

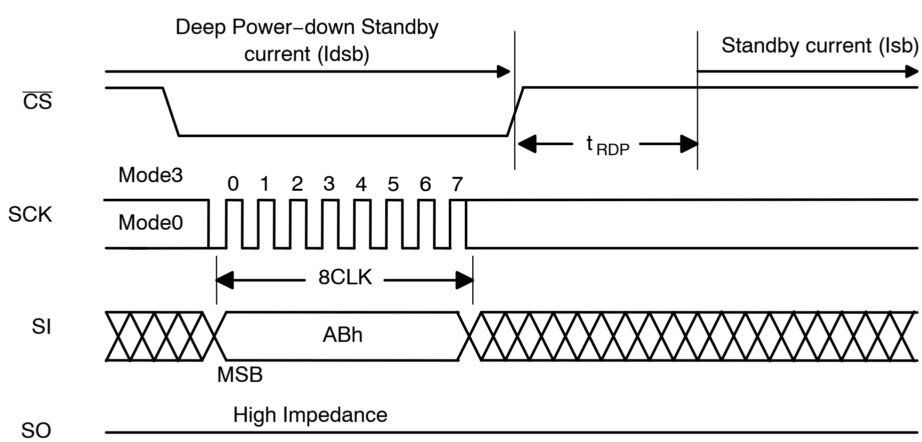


Figure 25. Exiting from Deep Power−down (EDP)

Read Device ID (RDDI)

Also the exit from deep power−down is completed by one byte cycle or more of the Read Device ID (RID: ABh).

"*Table 13. Device ID Code*" lists the device ID codes.

"*Figure 26. Read Device ID*" shows the timing waveforms.

The sequence of EDP & RID operation:

$\overline{CS}$ goes to low → input RID command (ABh) → 3 byte dummy cycle

→ Device ID out on SO →→

→ completed by $\overline{CS}$ = high

*The Device ID is output repeatedly as long as clock inputs are present

*The data output starts from the falling edge of SCK (31th clock)

By setting $\overline{CS}$ to high, the device is deselected, and Read ID cycle is completed. While the device is deselected, the output pin SO is in a high−impedance state.

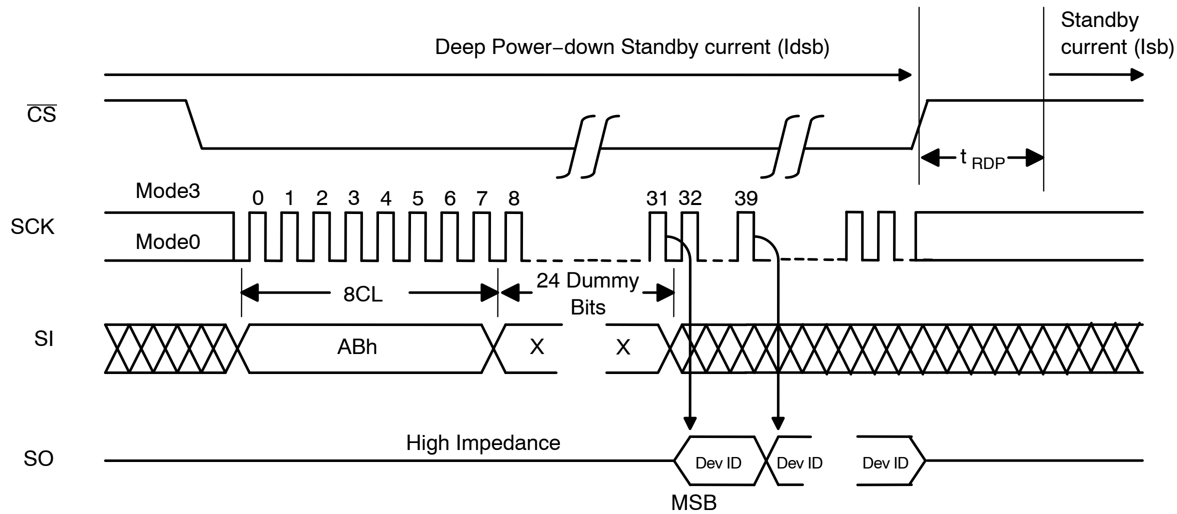


Figure 26. Read Device ID

Software Reset

The Software Reset reset the device to the state just after power−on. This operation consists of two commands: the Reset Enable (RSTEN) and the Reset command (RST).

"*Figure 27. Software Reset*" shows the timing waveforms.

The sequence of Software Reset operation:

$\overline{CS}$ goes to low → input RSTEN command (66h)

→ $\overline{CS}$ goes to high

→ $\overline{CS}$ goes to low → input RST command (99h)

→ $\overline{CS}$ goes to high (be executed by the rising $\overline{CS}$ edge)

When the Software Reset is executed, an internal write (erase/program) operation is cancel, a suspended status is reset, and all volatility status register bits (WEN/$\overline{RDY}$/SUS) are reset. After the internal reset time (tRST), the device will become stand−by state. If the Software Reset is executed during a write (erase/program) operation, any dates on the write operation will be broken.

The Reset command must input just after input the Reset Enable command. If another command input after the Reset Enable command, the Reset−Enable state will be invalid.

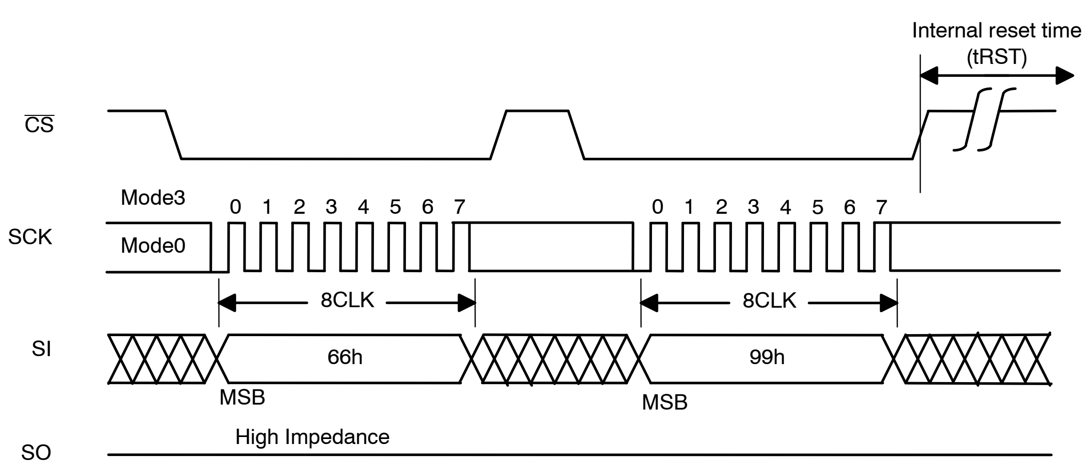


Figure 27. Software Reset

Read SFDP (RSFDP)

The Read SFDP (Serial Flash Discoverable Parameter) is an operation that reads the parameter about device configurations, available commands and other features. The SFDP parameters are stored in internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. SFDP is a standard of JEDEC. JESD216. Rev 1.0.

"*Table 14. SFDP Header*" shows SFDP Header.

"*Table 15. SFDP Parameter Table*" shows SFDP Parameter Table.

"*Figure 28. Read SFDP (RSFDP)*" shows the timing waveforms.

The sequence of RSFDP operation:

$\overline{\text{CS}}$ goes to low → input RSFDP command (5Ah) → 3 Byte address (A23 − A0) input on SI

→ 1 byte dummy cycle the corresponding parameter out on SO

→ continuous parameter out (n−byte) →→

→ completed by $\overline{\text{CS}}$ = high

*A10 to A0 are valid address

*The parameter output starts from the falling edge of SCK (39th clock)

The Address is latched on rising edge of SCK. It is necessary to add 1 dummy byte cycle after address is latched, and the corresponding parameter is shifted out on SO by the falling edge of SCK. The address is automatically incremented to the next higher address after each byte parameter is shifted out. By setting $\overline{\text{CS}}$ to high, the device is deselected, and Read SFDP cycle is completed. While the device is deselected, the output pin SO is in a high−impedance state.

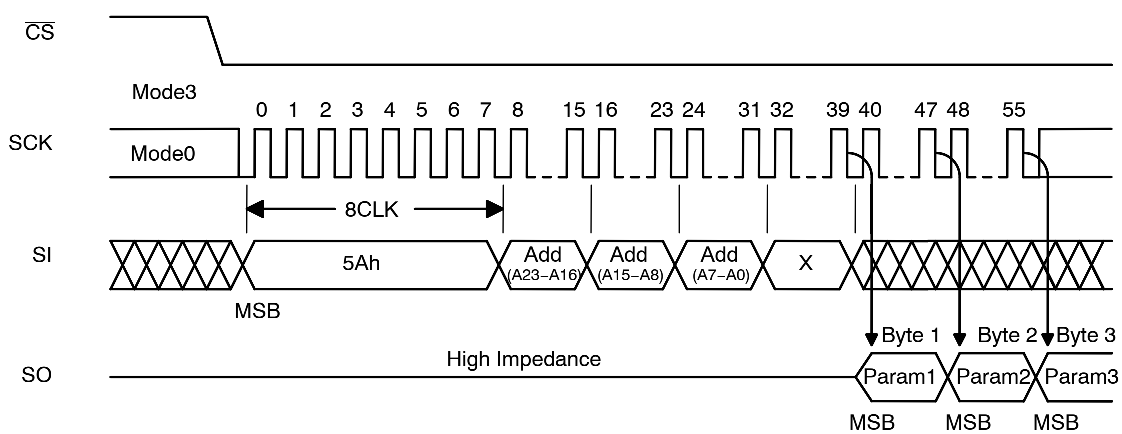


Figure 28. Read SFDP (RSFDP)

Table 14. SFDP HEADER

Description	Comment	Byte Address (Hex)	Bits	Data (Hex)
SFDP HEADER 1st AND 2nd DWORD				
SFDP Signature	50444653h (SFDP)	00h	7:0	53h
		01h	15:8	46h
		02h	23:16	44h
		03h	31:24	50h
SFDP Minor Revision Number	Start from 00h	04h	7:0	05h
SFDP Major Revision Number	Start from 01h	05h	15:8	01h
Number of Parameter Headers	02h indicates 3 parameters	06h	23:16	02h
Unused		07h	31:24	FFh
1st PARAMETER HEADER (JDEC BASIC FLASH PARAMETERS)				
ID Number (JEDEC ID)	00h (JEDEC specified header)	08h	7:0	00h
Parameter Table Minor Revision Number	Start from 00h	09h	15:8	00h
Parameter Table Major Revision Number	Start from 01h	0Ah	23:16	01h
Parameter Table Length (in Double Word)	How many DWORDs in the Parameter table 10h indicates 16 DWORDs	0Bh	31:24	10h
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0Ch	7:0	40h
		0Dh	15:8	00h
		0Eh	23:16	00h
Unused		0Fh	31:24	FFh
2nd PARAMETER HEADER (VENDER PARAMETERS 1)				
ID Number (**onsemi** Manufacturer ID)	62h (ON Semiconductor manufacturer ID)	10h	7:0	62h
Parameter Table Minor Revision Number	Start from 00h	11h	15:8	00h
Parameter Table Major Revision Number	Start from 01h	12h	23:16	01h
Parameter Table Length (in Double Word)	How many DWORDs in the Parameter table 04h indicates 4 DWORDs	13h	31:24	04h
Parameter Table Pointer (PTP)	First address of On Semiconductor Parameter table	14h	7:0	C0h
		15h	15:8	00h
		16h	23:16	00h
Unused		17h	31:24	FFh

Table 15. SFDP PARAMETER TABLE

Description	Comment	Byte Address (Hex)	Bits	Data (Binary)	Data (Hex)
JDEC Basic Flash Parameter Tables (from 1st DWORD TO 4th DWORD)					
Block/Sector Erase Sizes	00b: Reserved 01b: support 4 kB Erase 10b: Reserved 11b: not support 4 kB Erase	40h	1:0	01b	E5h
Write Granularity	0: 1 Byte, 1:64 Byte or larger		2	1b	
Volatile Status Register Block Protect Bits	0: Non−volatile 1: Volatile		3	0b	
Write Enable Instruction Select for Writing to Volatile Status Register	0: use 50h opcode, 1: use 06h opcode NOTE: If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b.		4	0b	
Unused	Contains 111b and can never be changed		7:5	111b	
4 kB Erase Instruction	20h	41h	15:8	0010_0000b	20h
(1−1−2) Fast Read	0 = not support 1 = support	42h	16	1b	91h
Address Bytes	00: 3 Byte only, 01: 3 or 4 Byte, 10: 4 Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) Clocking	0 = not support 1 = support		19	0b	
(1−2−2) Fast Read	0 = not support 1 = support		20	1b	
(1−4−4) Fast Read	0 = not support 1 = support		21	0b	
(1−1−4) Fast Read	0 = not support 1 = support		22	0b	
Unused			23	1b	
Unused		43h	31:24	1111_1111b	FFh
Flash Memory Density	16 M bits	44h 45h 46h 47h	31:0	−	00FFFFFFh
(1−4−4) Fast Read Number of Wait States (Dummy Clocks)	0 0000b: Wait states (dummy Clocks) not support	48h	4:0	0_0000b	00h
(1−4−4) Fast Read Number of Mode Clocks	000b: Mode Bits not support		7:5	000b	
(1−4−4) Fast Read Instruction		49h	15:8	1111_1111b	FFh
(1−1−4) Fast Read Number of Wait States (Dummy Clocks)	0 0000b: Wait states (dummy Clocks) not support	4Ah	20:16	0_0000b	00h
(1−1−4) Fast Read Number of Mode Clocks	000b: Mode Bits not support		23:21	000b	
(1−1−4) Fast Read Instruction		4Bh	31:24	1111_1111b	FFh
(1−1−2) Fast Read Number of Wait States (Dummy Clocks)	0 0000b: Wait states (dummy Clocks) not support	4Ch	4:0	0_1000b	08h
(1−1−2) Fast Read Number of Mode Clocks	000b: Mode Bits not support		7:5	000b	
(1−1−2) Fast Read Instruction		4Dh	15:8	0011_1011b	3Bh
(1−2−2) Fast Read Number of Wait States (Dummy Clocks)	0 0000b: Wait states (dummy Clocks) not support	4Eh	20:16	0_0100b	04h
(1−2−2) Fast Read Number of Mode Clocks	000b: Mode Bits not support		23:21	000b	
(1−2−2) Fast Read Instruction		4Fh	31:24	1011_1011b	BBh

Table 15. SFDP PARAMETER TABLE (continued)

Description	Comment	Byte Address (Hex)	Bits	Data (Binary)	Data (Hex)
JDEC BASIC FLASH PARAMETER TABLES (FROM 5th DWORD TO 8th DWORD)					
(2–2–2) Fast Read	0 = not support 1 = support	50h	0	0b	EEh
Reserved	Default all 1’s		3:1	111b	
(4–4–4) Fast Read	0 = not support 1 = support		4	0b	
Reserved	Default all 1’s		7:5	111b	
Reserved	Default all 1’s	51h 52h 53h	31:8	–	FFh FFh FFh
Reserved	Default all 1’s	54h 55h	15:0	–	FFh FFh
(2–2–2) Fast Read Number of Wait states (Dummy Clocks)	0 0000b: Wait states (dummy Clocks) not support	56h	20:16	0_0000b	00h
(2–2–2) Fast Read Number of Mode Clocks	000b: Mode Bits not support		23:21	000b	
(2–2–2) Fast Read Instruction		57h	31:24	1111_1111b	FFh
Reserved	Default all 1’s	58h 59h	15:0	–	FFh FFh
(4–4–4) Fast Read Number of Wait States (Dummy Clocks)	0 0000b: Wait states (dummy Clocks) not support	5Ah	20:16	0_0000b	00h
(4–4–4) Fast Read Number of Mode Clocks	000b: Mode Bits not support		23:21	000b	
(4–4–4) Fast Read Instruction		5Bh	31:24	1111_1111b	FFh
Sector Type 1 Size	Sector/block size = 2^N bytes 0Ch indicates 4 kbytes	5Ch	7:0	0000_1100b	0Ch
Sector Type 1 Erase Instruction		5Dh	15:8	0010_0000b	20h
Sector Type 2 Size	Sector/block size = 2^N bytes 10h indicates 64 kbytes	5Eh	23:16	0001_0000b	10h
Sector Type 2 Erase Instruction		5Fh	31:24	1101_1000b	D8h
JDEC BASIC FLASH PARAMETER TABLES (FROM 9th DWORD TO 12th DWORD)					
Sector Type 3 Size	Sector/block size = 2^N bytes 00h indicates not exist	60h	7:0	0000_0000b	00h
Sector Type 3 Erase Instruction		61h	15:8	1111_1111b	FFh
Sector Type 4 Size	Sector/block size = 2^N bytes 00h indicates not exist	62h	23:16	0000_0000b	00h
Sector Type 4 Erase Instruction		63h	31:24	1111_1111b	FFh
Multiplier from Typical Erase Time to Maximum Erase Time	SE (64 k–Byte erase): 150 ms = 2 x (n + 1) x 15 ms n = 4	64h	3:0	0100b	94h
Sector Type 1 Erase, Typical Time	SSE (4 k–Byte erase) 10 ms: ((n + 1) x 1 ms = 10 ms) n = 9	65h	10:4	00_01001b	70h
Sector Type 2 Erase, Typical Time	SE (64 k–Byte erase) 15 ms: ((n + 1) x 1 ms = 15 ms) n = 14	66h	17:11	00_01110b	00h
Sector Type 3 Erase, Typical Time	–	67h	24:18	00_00000b	00h
Sector Type 4 Erase, Typical Time	–		31:25	00_00000b	

Table 15. SFDP PARAMETER TABLE (continued)

Description	Comment	Byte Address (Hex)	Bits	Data (Binary)	Data (Hex)
JDEC BASIC FLASH PARAMETER TABLES (FROM 9th DWORD TO 12th DWORD)					
Multiplier from Typical Time to Max Time for Page or Byte Program	(n + 1) x 0.3 ms = 0.9 ms: n = 2, 0.9 ms > 0.7 ms (spec)	68h	3:0	0010b	82h
Page Size	256 Bytes =2^8		7:4	1000b	
Page Program Typical Time	(n + 1) x 64 µs = 448 µs: n = 6, 448 µs > 400 µs (spec)	69h	13:8	1_00110b	E6h
Byte Program Typical Time, First Byte	(n + 1) x 8 µs = 128 µs: n = 15		15:14	1_1111b	
		6Ah	18:16		07h
Byte Program Typical Time, Additional Byte	(count + 1) x 1 µs/byte = 1 µs/byte: Count = 0		23:19	0_0000b	
Chip Erase, Typical Time	(n + 1) x 16 ms = 208 ms: n = 12, 208 ms = 210 ms (spec)	6Bh	30:24	00_01100b	0Ch
Reserved	–		31	0b	
Prohibited Operations During Program Suspend	xxx0b: May not initiate a new erase anywhere xxx1b: May not initiate a new erase in the program suspended page size xx0xb: May not initiate a new page program anywhere xx1xb: May not initiate a new page program in the program suspended page size x0xxb: Refer to vendor datasheet for read restrictions x1xxb: May not initiate a read in the program suspended page size 0xxxb: Additional erase or program restrictions apply 1xxxb: The erase and program restrictions in bits 1:0 are sufficient	6Ch	3:0	1101b	FDh
Prohibited Operations During Erase Suspend	xxx0b: May not initiate a new erase anywhere xxx1b: May not initiate a new erase in the erase suspended sector size xx0xb: May not initiate a page program anywhere xx1xb: May not initiate a page program in the erase suspended sector size x0xxb: Refer to vendor datasheet for read restrictions x1xxb: May not initiate a read in the erase suspended sector size 0xxxb: Additional erase or program restrictions apply 1xxxb: The erase and program restrictions in bits 5:4 are sufficient		7:4	1111b	
Reserved	–	6Dh	8	0b	80h
Program Resume to Suspend Interval	<64 µs: (count + 1) x 64 µs, count = 0		12:9	0000b	
Suspend In–progress Program Max Latency	40 µs: ((4 + 1) x 8 µs = 40 µs)		15:13	10_00100b	
		6Eh	19:16		08h
Erase Resume to Suspend Interval	<64 µs: (count + 1) x 64 µs, count = 0		23:20	0000b	
Suspend In–progress Erase Max Latency	40 µs: ((4 + 1) x 8 µs = 40 µs)	6Fh	30:24	10_00100b	44h
Suspend/Resume Supported	0 = support 1 = not support		31	0b	

Table 15. SFDP PARAMETER TABLE (continued)

Description	Comment	Byte Address (Hex)	Bits	Data (Binary)	Data (Hex)
JDEC BASIC FLASH PARAMETER TABLES (FROM 13th DWORD TO 16th DWORD)					
Program Resume Instruction (Program Operation)	30h (as same as erase resume)	70h	7:0	0011_0000b	30h
Program Suspend Instruction (Program Operation)	B0h (as same as erase suspend)	71h	15:8	1011_0000b	B0h
Resume Instruction (Write or Erase Type Operation)	30h (as same as program resume)	72h	23:16	0011_0000b	30h
Suspend Instruction (Write or Erase Type Operation)	B0h (as same as program suspend)	73h	31:24	1011_0000b	B0h
Reserved		74h	1:0	00b	04h
Status Register Polling Device Busy	Use legacy polling by reading the Status Register with 05h instruction		7:2	0000_01b	
Exit Deep Power Down to Next Operation Delay	40 µs: ((4+1) x 8 µs = 40 µs)	75h	14:8	10_00100b	C4h
Exit Deep Power Down Instruction	ABh		15	1010_1011b	
		76h	22:16		D5h
Enter Deep Power Down Instruction	B9h		23	1011_1001b	
		77h	30:24		5Ch
Deep Power Down Supported	0 = support 1 = not support		31	0b	
(4−4−4) Mode Disable Sequences	–	78h	3:0	0000b	00h
(4−4−4) Mode Enable Sequences	–		7:4	0000b	
		79h	8	0b	00h
(0−4−4) Mode Supported	0 = not support 1 = support		9	0b	
(0−4−4) Mode Exit Method	–		15:10	00_0000b	
(0−4−4) Mode Entry Method	–	7Ah	19:16	0000b	00h
Quad Enable Requirements (QER)	00b: not have a QE bit		22:20	000b	
Hold and WP Disable	0: not supported		23	0b	
Reserved	–	7Bh	31:24	0000_0000b	00h
Volatile or Non−Volatile Register and Write Enable Instruction for Status Register 1	xxx_xxx1b: Non−Volatile Status Register 1, powers−up to last written value, use instruction 06h to enable write xx1_xxxxb: Status Register 1 contains a mix of volatile and non−volatile bits. The 06h instruction is used to enable writing of the register.	7Ch	6:0	001_1001b	19h
Reserved	–		7	0b	
Soft Reset and Rescue Sequence Support	Issue reset enable instruction 66h, and then issue reset instruction 99h.	7Dh	13:8	01_0000b	10h
Exit 4−Byte Addressing			15:14	00b	
		7Eh	23:16	0000_0000b	00h
Enter 4−Byte Addressing		7Fh	31:24	0000_0000b	00h

Table 15. SFDP PARAMETER TABLE (continued)

Description	Comment	Byte Address (Hex)	Bits	Data (Binary)	Data (Hex)
VENDER (ON SEMICONDUCTOR) PARAMETER 1 TABLES (FROM 1th DWORD TO 4th DWORD)					
Supply Maximum Voltage	1900h = 1.900 V 1950h = 1.950 V 2000h = 2.000 V 2200h = 2.200 V 2400h = 2.400 V 2700h = 2.700 V 3000h = 3.000 V 3600h = 3.600 V	C0h C1h	15:0	–	50h 19h
Supply Minimum Voltage	1600h = 1.600 V 1650h = 1.650 V 1700h = 1.700 V 1800h = 1.800 V 20000h = 2.000 V 22000h = 2.200 V 23000h = 2.300 V 27000h = 2.700 V	C2h C3h	31:16	–	50h 16h
RESET Pin	0 = not support 1 = support	C4h	0	0b	14h
RESET Active Logic Level	0 = active logic is 0 1 = active logic is 1		1	0b	
HOLD Pin	0 = not support 1 = support		2	1b	
HOLD Active Logic Level	0 = active logic is 0 1 = active logic is 1		3	0b	
WP Pin	0 = not support 1 = support		4	1b	
WP Active Logic Level	0 = active logic is 0 1 = active logic is 1		5	0b	
Reserved	00b		7:6	00b	
Reserved	All FFh	C5h C6h C7h	31:8	1111_1111b 1111_1111b 1111_1111b	FFh FFh FFh
JDEC ID Operation Code	9Fh	C8h	7:0	1001_1111b	9Fh
JDEC ID Read Data (Manufacture Code)	62h (ON Semiconductor)	C9h	15:8	0110_0010b	62h
JDEC ID Read Data (Memory Type)	16h	CAh	23:16	0001_0110b	16h
JDEC ID Read Data (Memory Capacity Code)	15h (16 Mbits)	CBh	31:24	0001_0101b	15h
Device ID Operation Code	ABh	CCh	7:0	1010_1011b	ABh
Device ID Read Data	88h (LE25S161)	CDh	15:8	1000_1000b	88h
Reserved	All FFh	CEh CFh	31:16	1111_1111b 1111_1111b	FFh FFh

HOLD FUNCTION

Using the $\overline{HOLD}$ pin, the hold function suspends serial communication (it places it in the hold status). "*Figure 29. $\overline{HOLD}$ Function*" shows the timing waveforms. The device is placed in the hold status at the falling $\overline{HOLD}$ edge while the logic level of SCK is low, and it exits from the hold status at the rising $\overline{HOLD}$ edge. When the logic level of SCK is high, $\overline{HOLD}$ must not rise or fall. The hold function takes effect when the logic level of $\overline{CS}$ is low, the hold status is exited and serial communication is reset at the rising $\overline{CS}$ edge. In the hold status, the SO output is in the high−impedance state, and SI and SCK are "don't care".

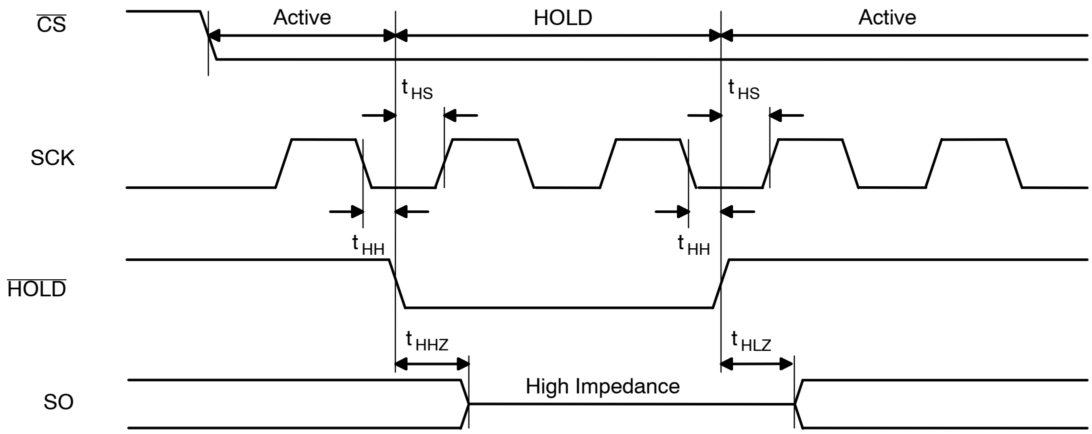


Figure 29. HOLD Function

POWER−ON

In order to protect against unintentional writing, $\overline{CS}$ must be within at V_{DD}−0.3 to V_{DD}+0.3 on power−on. After power−on, the supply voltage has stabilized at V_{DD} (min) or higher, and waits for t_{VSL} before $\overline{CS}$ is driven to "Low".

The device is in the standby state after power is turned on.

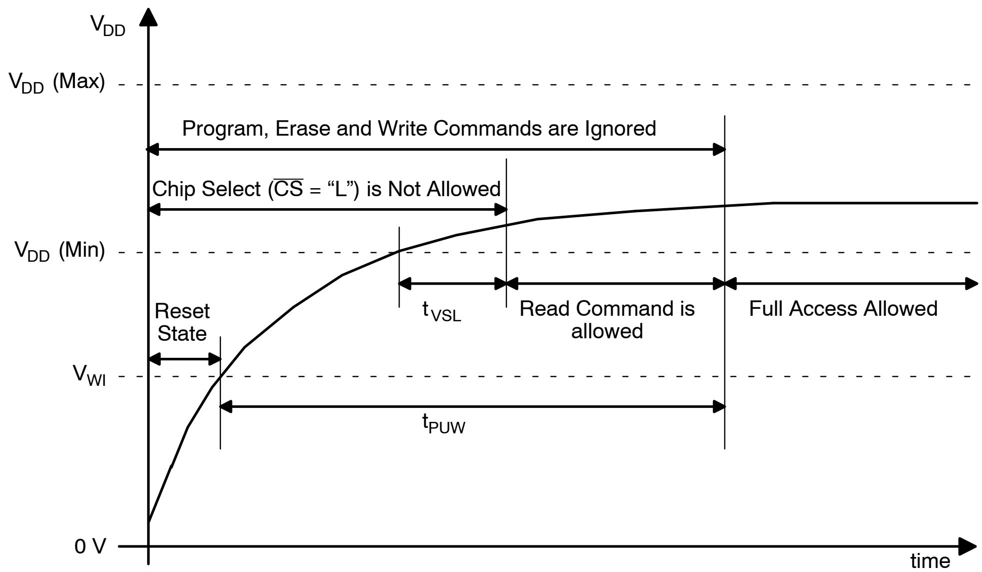


Figure 30. Power−on Timing

Table 16. POWER−UP TIMING

Parameter	Symbol	Spec		Unit
		Min	Max	
V_{DD}(Min) to $\overline{CS}$ Low	t_{VSL}	300	–	µs
Time to Write Operation	t_{PUW}	100	500	µs
Operation Inhibit Voltage	V_{WI}	1.0	1.5	V

HARDWARE DATA PROTECTION

LE25S161 incorporates a power−on reset function. The following conditions must be met in order to ensure that the power reset circuit will operate stably.

No guarantees are given for data in the event of an instantaneous power failure occurring during the writing period.

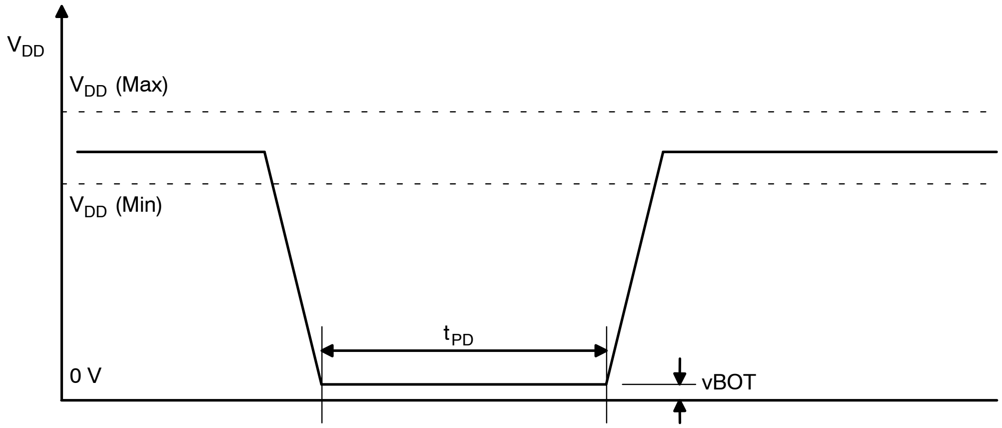


Figure 31. Power−down Timing

Table 17. POWER−DOWN TIMING

Parameter	Symbol	Spec		Unit
		Min	Max	
Power−down Time	t_{PD}	10	–	ms
Power−down Voltage	V_{BOT}	–	0.2	V

SOFTWARE DATA PROTECTION

The LE25S161 eliminates the possibility of unintentional operations by not recognizing commands under the following conditions.

- When a write command is input and the rising $\overline{CS}$ edge timing is not in a byte cycle (8 CLK units of SCK)
- When the Page Program data is not in 1−byte increments
- When the Write Status Register command is input for 2 bytes cycles or more

DECOUPLING CAPACITOR

0.1 μF ceramic capacitor must be provided to each device and connected between V_{DD} and V_{SS} in order to ensure that the device will operate stably.

SPECIFICATIONS

Absolute Maximum Ratings

Table 18. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Maximum Supply Voltage		With respect to V_{SS}	–0.5 to +2.6	V
DC Voltage (All Pins)		With respect to V_{SS}	–0.5 to V_{DD} + 0.5	V
Storage Temperature	Tstg		–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Operating Conditions

Table 19. OPERATING CONDITIONS

Parameter	Symbol	Conditions	Rating	Unit
Operating Supply Voltage			1.65 to 1.95	V
Operating Ambient Temperature			–40 to +90	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Data Retention, Rewriting Cycles

Table 20. DATA RETENTION, REWRITING CYCLES

Parameter	Symbol	Conditions	Min	Max	Unit
Rewrite Cycles	cycRW	Status resister write	100,000	–	cycles/ Sector
		Program/Erase	100,000	–	
Data Retention	tDRET		20	–	year

Pin Capacitance at Ta = 25°C, f = 1 MHz

Table 21. PIN CAPACITANCE (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Rating	Unit
			Max	
Output Pin Capacitance	C_{SO}	V_{SO} = 0 V	12	pF
Input Pin Capacitance	C_{IN}	V_{IN} = 0 V	6	pF

NOTE: These parameter values do not represent the results of measurements undertaken for all devices but rather values for some of the sampled devices.

AC Test Conditions

Input pulse level	0.2 V_{DD} to 0.8 V_{DD}
Input rising/falling time	5 ns
Input timing level	0.3 V_{DD}, 0.7 V_{DD}
Output timing level	1/2 x V_{DD}
Output load	15 pF

NOTE: As the test conditions for “typ”, the measurements are conducted using 1.8 V for V_{DD} at room temperature.

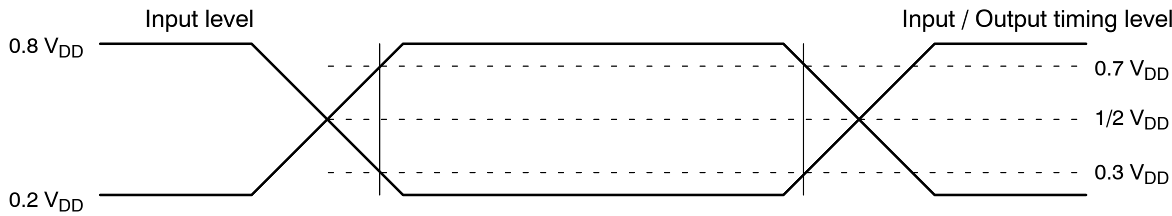


Figure 32.

DC Characteristics

Table 22. DC CHARACTERISTICS

Parameter	Symbol	Conditions			V_{DD} = 1.65 to 1.95 V Rating Min	Typ	Max	Unit
Read Mode Operating Current	I_{CCR}	SCK = 0.1 V_{DD} / 0.9 V_{DD}, $\overline{HOLD}$ = $\overline{WP}$ = 0.9 V_{DD}, SO = open	Low−Power Read (RDLP: 03h)	33.33 MHz	–	3.5	4.5	mA
			High−Speed Read (RDHS: 0Bh)	33.33 MHz	–	4.0	5.5	
				70 MHz	–	6.0	7.0	
			Dual Output Read (RDDO: 3Bh) or Dual I/O Read (RDIO: BBh)	33.33 MHz	–	5.0	7.0	
				50 MHz	–	6.0	7.0	
Small Sector Erase Operating Current	I_{CCSSE}	t_{SSE}=max Average current			–	3.5	4.5	mA
Sector Erase Operating Current	I_{CCSE}	t_{SE}=max Average current			–	3.5	4.5	mA
Chip Erase Operating Current	I_{CCCHE}	t_{CHE}=max Average current			–	4.0	5.0	mA
Normal Program Mode Operating Current	I_{CCPP}	t_{PP}=max Average current			–	6.5	7.5	mA
Low−Power Program Mode Operating Current	I_{CCPPL}	t_{PPL}=max Average current			–	5.0	6.5	mA
CMOS Standby Current	I_{SB}	$\overline{CS}$ = V_{DD}, $\overline{HOLD}$ = $\overline{WP}$ = V_{DD}, SI = VSS / V_{DD}, SO = open			–	9	50	μA
Deep Power−down Standby Current	I_{DSB}	$\overline{CS}$ = V_{DD}, $\overline{HOLD}$ = $\overline{WP}$ = V_{DD}, SI = VSS / V_{DD}, SO = open			–	3.0	12	μA
Input Leakage Current	I_{LI}				–	–	2.0	μA
Output Leakage Current	I_{LO}				–	–	2.0	μA
Input Low Voltage	V_{IL}				−0.3	–	0.3 V_{DD}	V
Input High Voltage	V_{IH}				0.7 V_{DD}	–	V_{DD} + 0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 100 μA, V_{DD} = V_{DD} min			–	–	0.2	V
		I_{OL} = 1.6 mA, V_{DD} = V_{DD} min			–	–	0.4	
Output High Voltage	V_{OH}	I_{OH} = −100 μA, V_{DD} = V_{DD} min			V_{DD} − 0.2	–	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC Characteristics

Table 23. AC CHARACTERISTICS

Parameter		Symbol	Rating Min	Rating Typ	Rating Max	Unit
Clock Frequency	Low−Power Read (RDLP: 03h)	f_{CLK}	–	–	33.33	MHz
	Dual Output Read (RDDO: 3Bh) Dual I/O Read (RDIO: BBh)		–	–	50	
	Other Instructions		–	–	70	
Input Signal Rising/Falling Time		t_{RF}	0.1	–	–	V/ns
SCK Logic High Level Pulse Width	33.33 MHz	t_{CLHI}	11	–	–	ns
	50 MHz		8	–	–	
	70 MHz		6	–	–	
SCK Logic Low Level Pulse Width	33.33 MHz	t_{CLLO}	11	–	–	ns
	50 MHz		8	–	–	
	70 MHz		6	–	–	
$\overline{CS}$ Active Setup Time		t_{SLCH}	6	–	–	ns
$\overline{CS}$ Not Active Hold Time		t_{CHSL}	6	–	–	ns
Data Setup Time		t_{DS}	3	–	–	ns
Data Hold Time		t_{DH}	3	–	–	ns
$\overline{CS}$ Wait Pulse Width		t_{CPH}	20	–	–	ns
$\overline{CS}$ Active Hold Time		t_{CHSH}	6	–	–	ns
$\overline{CS}$ Not Active Setup Time		t_{SHCH}	6	–	–	ns
Output High Impedance Time from $\overline{CS}$		t_{CHZ}	–	–	8	ns
Output Data Time from SCK	33.33 MHz	t_V	–	–	10	ns
	50 MHz		–	–	8	
	70 MHz		–	–	8	
Output Data Hold Time		t_{HO}	1	–	–	ns
Output Low Impedance Time from SCK		t_{CLZ}	0	–	–	ns
$\overline{HOLD}$ Setup Time		t_{HS}	6	–	–	ns
$\overline{HOLD}$ Hold Time		t_{HH}	6	–	–	ns
Output Low Impedance Time from $\overline{HOLD}$		t_{HLZ}	–	–	8	ns
Output High Impedance Time from $\overline{HOLD}$		t_{HHZ}	–	–	8	ns
$\overline{WP}$ Setup Time		t_{WPS}	20	–	–	ns
$\overline{WP}$ Hold Time		t_{WPH}	20	–	–	ns
Write Status Register Time		t_{WRSR}	–	5	8	ms
Normal Page Programming Cycle Time	256 Byte	t_{PP}	–	0.40	0.70	ms
	nByte		–	0.14 + n x 0.26 / 256	0.35 + n x 0.35 / 256	
Low−Power Page Programming Cycle Time	256 Byte	t_{PPL}	–	0.60	1.20	ms
	nByte		–	0.14 + n x 0.46 / 256	0.50 + n x 0.70 / 256	
Small Sector Erase Cycle Time		t_{SSE}	–	10	120	ms
Sector Erase Cycle Time		t_{SE}	–	15	150	ms
Chip Erase Cycle Time		t_{CHE}	–	210	2400	ms
Recovery Time from Suspend		t_{RSUS}	–	–	40	μs
Deep Power−down Time		t_{DP}	–	–	5	μs
Deep Power−down Recovery Time		t_{RDP}	–	–	40	μs
Internal Reset Time		tRST	–	–	40	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TIMING WAVEFORMS

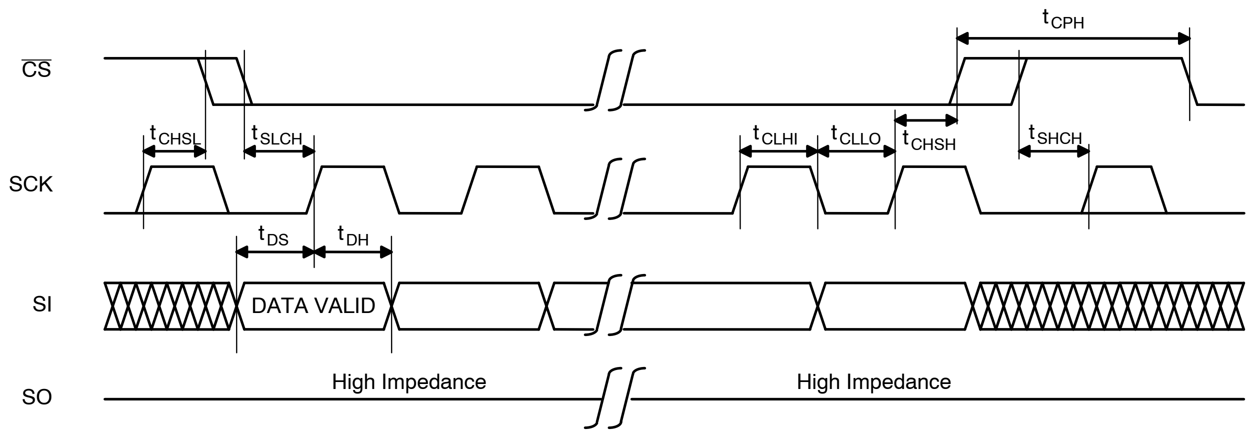


Figure 33. Serial Input Timing

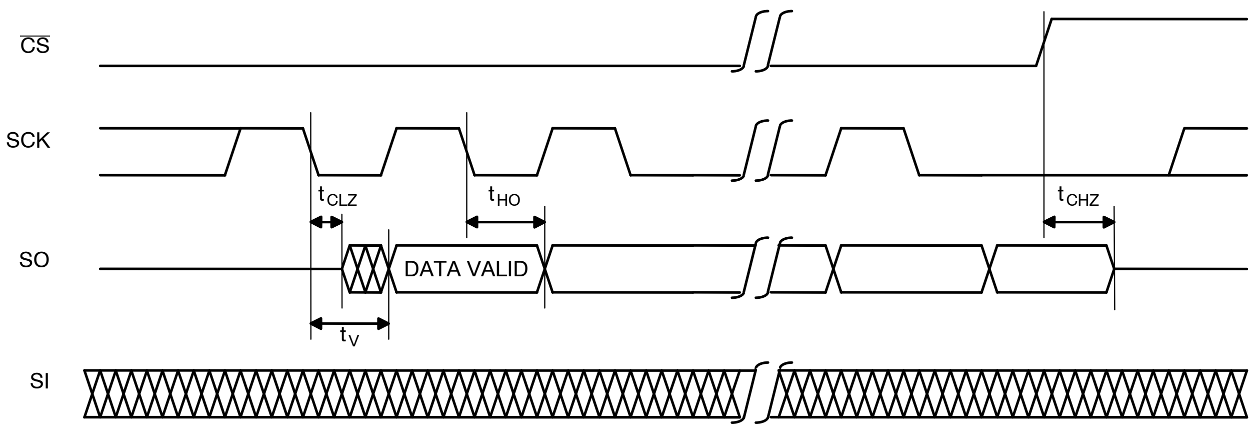


Figure 34. Serial Output Timing

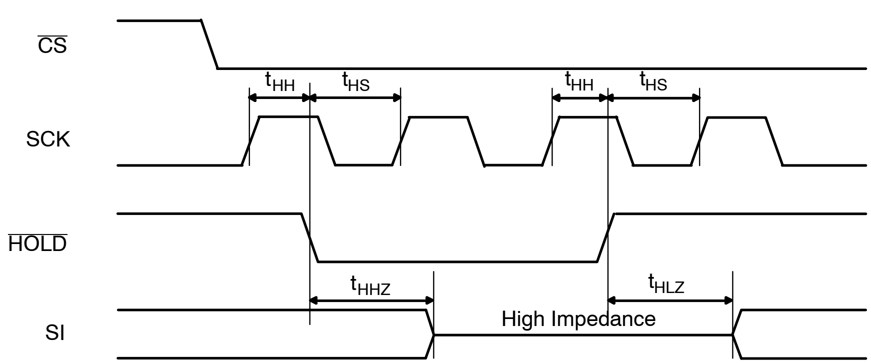


Figure 35. Hold Timing

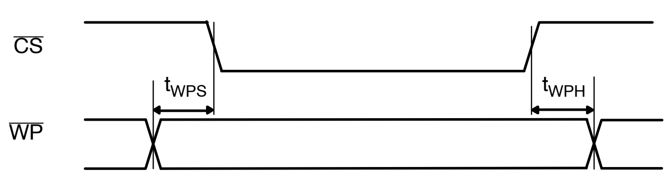


Figure 36. Status Resister Write Timing

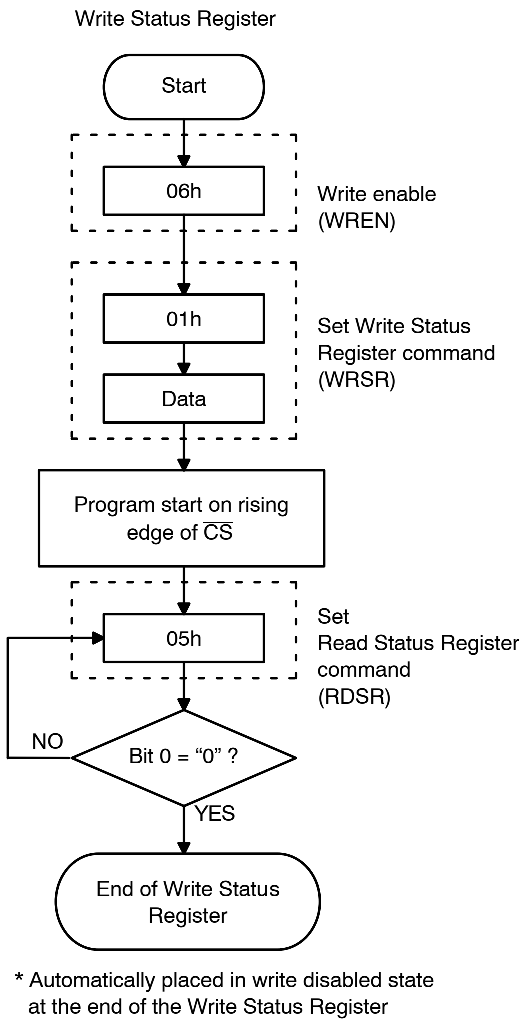


Figure 37. Write Status Register Flowcharts

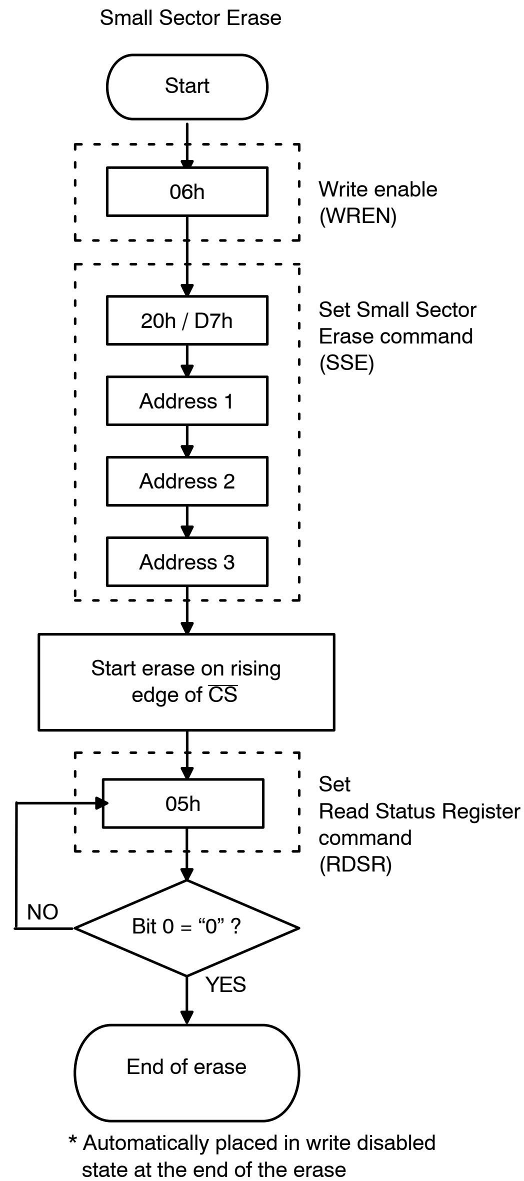


Figure 38. Small Sector Erase Flowcharts

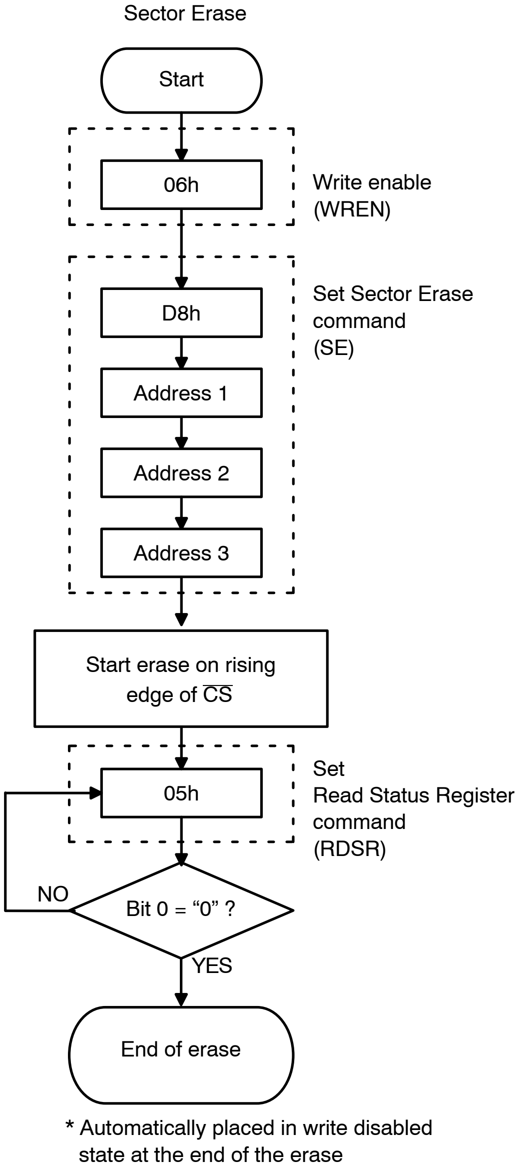


Figure 39. Sector Erase Flowcharts

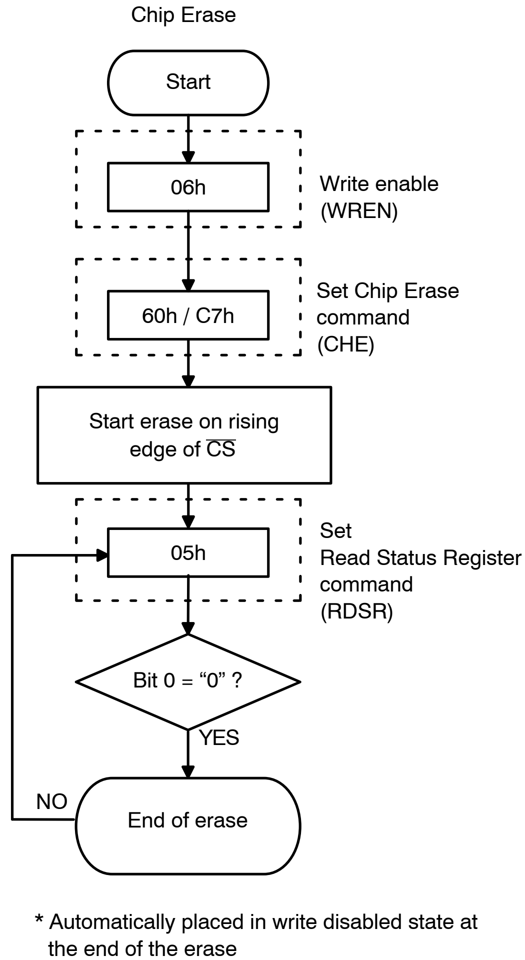
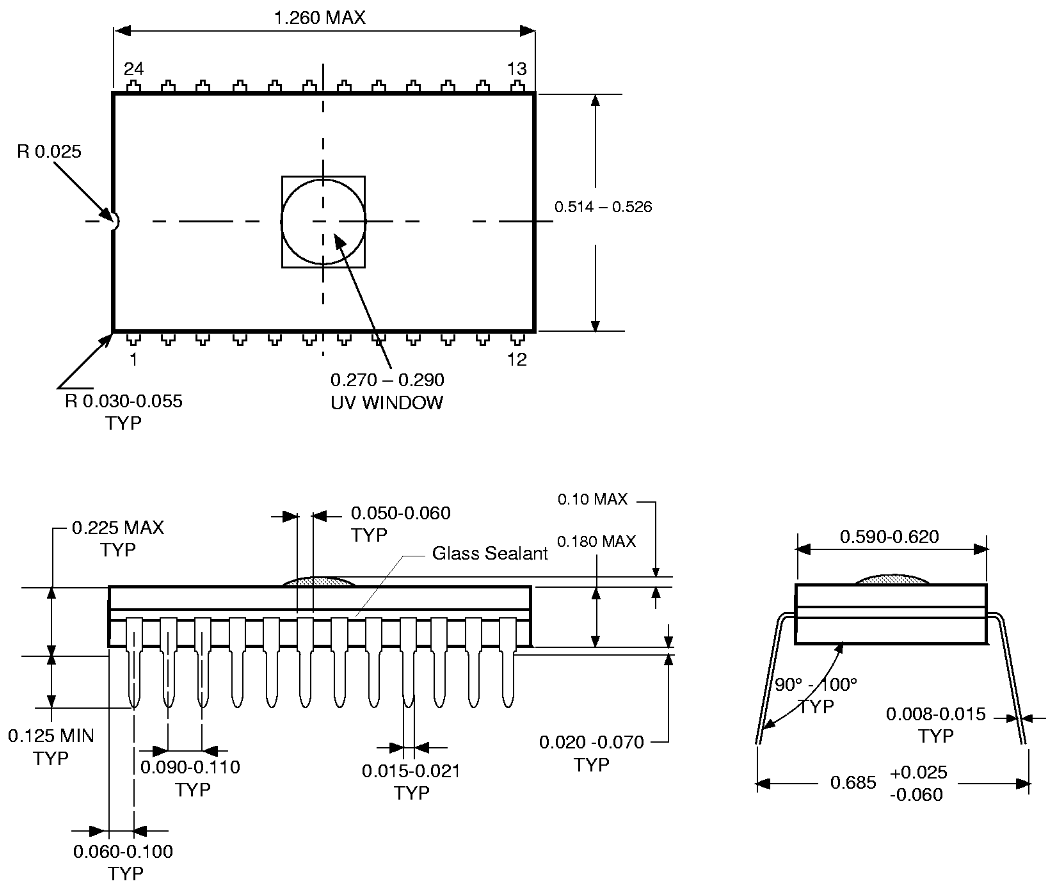


Figure 40. Chip Erase Flowcharts

Physical Dimensions inches (millimeters) unless otherwise noted



UV Window Cavity Dual-In-Line Cerdip Package (JQ)
Order Number NMC27C32BQ
Package Number J24AQ

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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