Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	—0.5V to +7.0V
V_I	DC Input Voltage	—0.5V to +7.0V
V_O	DC Output Voltage	
	Output in 3-STATE	—0.5V to +7.0V
	Output in HIGH or LOW State(4)	—0.5V to V_{CC} + 0.5V
I_{IK}	DC Input Diode Current, V_I < GND	—50mA
I_{OK}	DC Output Diode Current	
	V_O < GND	—50mA
	V_O > V_{CC}	+50mA
I_O	DC Output Source/Sink Current	–50mA
I_{CC}	DC Supply Current per Supply Pin	–100mA
I_{GND}	DC Ground Current per Ground Pin	–100mA
T_{STG}	Storage Temperature	—65¡C to +150¡C

Note:
4. I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions (5)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage			
	Operating	2.0	3.6	V
	Data Retention	1.5	3.6	
V_I	Input Voltage	0	5.5	V
V_O	Output Voltage			
	3-STATE	0	5.5	V
	HIGH or LOW State	0	V_{CC}	
I_{OH} / I_{OL}	Output Current			
	V_{CC} = 3.0V—3.6V		–24	mA
	V_{CC} = 2.7V—3.0V		–12	
	V_{CC} = 2.3V—2.7V		–8	
T_A	Free-Air Operating Temperature	—40	85	¡C
t / V	Input Edge Rate, V_{IN} = 0.8V—2.0V, V_{CC} = 3.0V	0	10	ns/V

Note:
5. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = —40¡C to +85¡C		Units
				Min.	Max.	
V_{IH}	HIGH Level Input Voltage	2.3—2.7		1.7		V
		2.7—3.6		2.0		
V_{IL}	LOW Level Input Voltage	2.3—2.7			0.7	V
		2.7—3.6			0.8	
V_{OH}	HIGH Level Output Voltage	2.3—3.6	I_{OH} = —100µA	V_{CC} — 0.2		V
		2.3	I_{OH} = —8mA	1.8		
		2.7	I_{OH} = —12mA	2.2		
		3.0	I_{OH} = —18mA	2.4		
			I_{OH} = —24mA	2.2		
V_{OL}	LOW Level Output Voltage	2.3—3.6	I_{OL} = 100µA		0.2	V
		2.3	I_{OL} = 8mA		0.6	
		2.7	I_{OL} = 12mA		0.4	
		3.0	I_{OL} = 16mA		0.4	
			I_{OL} = 24mA		0.55	
I_I	Input Leakage Current	2.3—3.6	0 V_I 5.5V		–5.0	µA
I_{OZ}	3-STATE Output Leakage	2.3—3.6	0 V_O 5.5V, $V_I = V_{IH}$ or V_{IL}		–5.0	µA
I_{OFF}	Power-Off Leakage Current	0	V_I or V_O = 5.5V		10	µA
I_{CC}	Quiescent Supply Current	2.3—3.6	$V_I = V_{CC}$ or GND		10	µA
			3.6V V_I, V_O 5.5V[6]		–10	
I_{CC}	Increase in I_{CC} per Input	2.3—3.6	$V_{IH} = V_{CC}$ — 0.6V		500	µA

Note:
6. Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	T_A = —40¡C to +85¡C, R_L = 500						Units
		V_{CC} = 3.3V – 0.3V, C_L = 50pF		V_{CC} = 2.7V, C_L = 50pF		V_{CC} = 2.5V – 0.2V, C_L = 30pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay, A_n to B_n or B_n to A_n	1.5	7.0	1.5	8.0	1.5	8.4	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.5	7.5	1.5	8.5	1.5	9.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew[7]		1.0					ns

Note:
7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25¡C$ Typical	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	0.8	V
		2.5	C_L = 30pF, V_{IH} = 2.5V, V_{IL} = 0V	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	3.3	C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V	—0.8	V
		2.5	C_L = 30pF, V_{IH} = 2.5V, V_{IL} = 0V	—0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7.0	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8.0	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, f = 10MHz	25.0	pF

AC Loading and Waveforms (Generic for LCX Family)

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 – 0.3V V_{CC} x 2 at V_{CC} = 2.5 – 0.2V
t_{PZH}, t_{PHZ}	GND

Figure 1. AC Test Circuit (C_L includes probe and jig capacitance)

Waveform for Inverting and Non-Inverting Functions

3-STATE Output High Enable and Disable Times for Logic

Propagation Delay. Pulse Width and t_{rec} Waveforms

Setup Time, Hold Time and Recovery Time for Logic

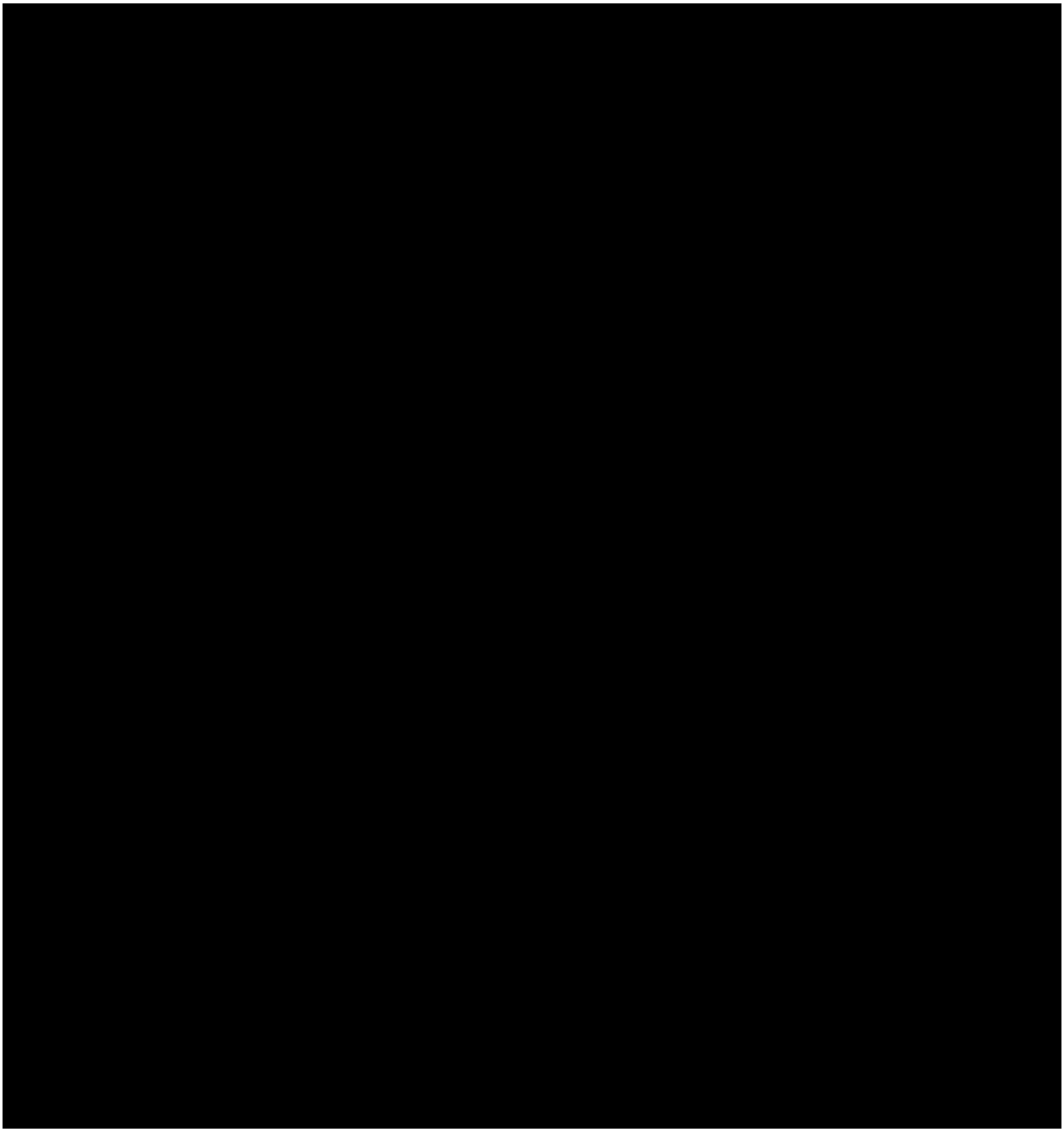
3-STATE Output Low Enable and Disable Times for Logic

t_{rise} and t_{fall}

Symbol	V_{CC}		
	3.3V – 0.3V	2.7V	2.5V – 0.2V
V_{mi}	1.5V	1.5V	V_{CC} / 2
V_{mo}	1.5V	1.5V	V_{CC} / 2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} — 0.3V	V_{OH} — 0.3V	V_{OH} — 0.15V

Figure 2. Waveforms (Input Characteristics; f = 1MHz, $t_r = t_f$ = 3ns)

Schematic Diagram (Generic for LCX Family)

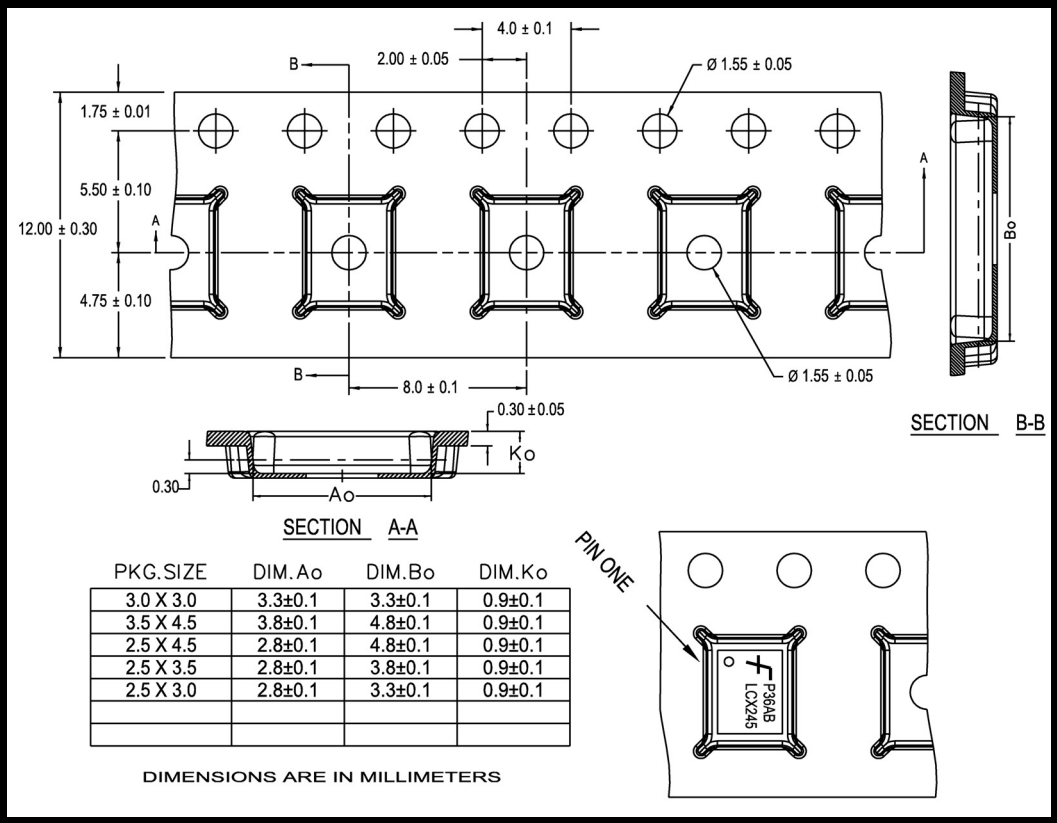


Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

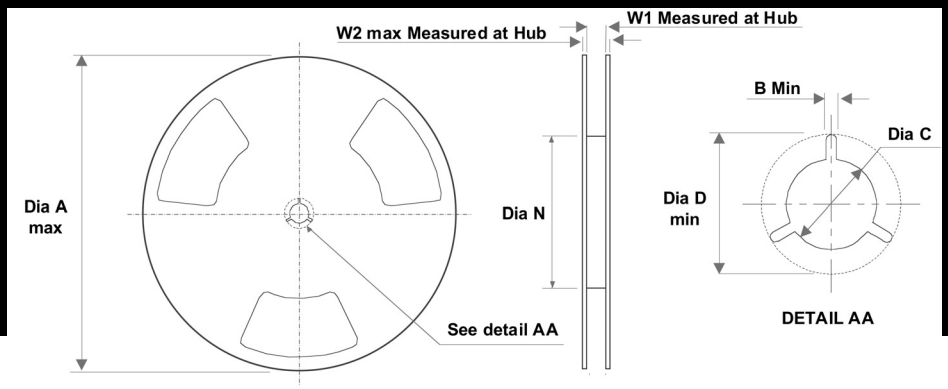
Tape Dimension inches (millimeters)



PKG.SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.0 X 3.0	3.3±0.1	3.3±0.1	0.9±0.1
3.5 X 4.5	3.8±0.1	4.8±0.1	0.9±0.1
2.5 X 4.5	2.8±0.1	4.8±0.1	0.9±0.1
2.5 X 3.5	2.8±0.1	3.8±0.1	0.9±0.1
2.5 X 3.0	2.8±0.1	3.3±0.1	0.9±0.1

DIMENSIONS ARE IN MILLIMETERS

Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12mm	13.0 (330.0)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.488 (12.4)	0.724 (18.4)

Physical Dimensions

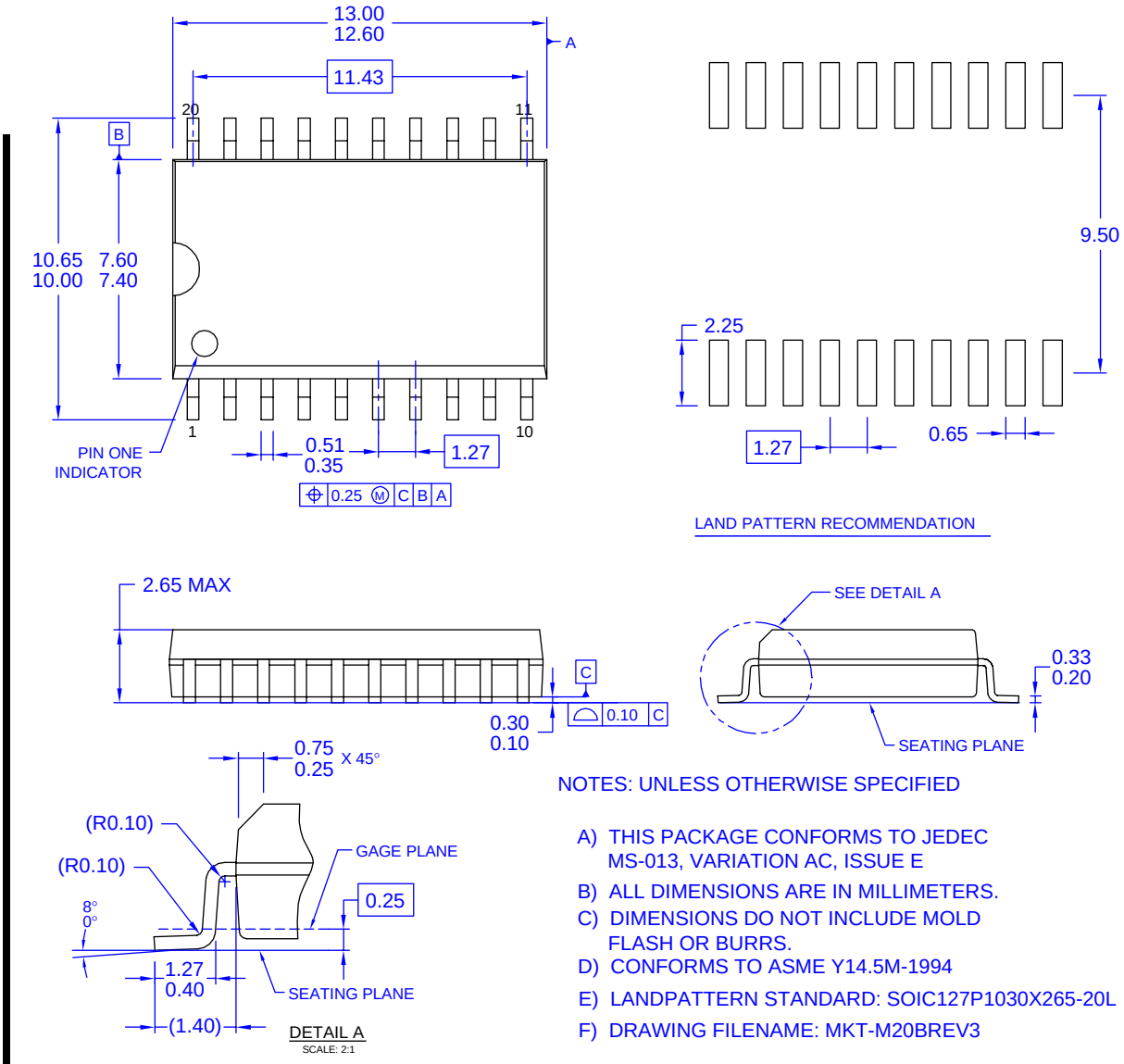


Figure 3. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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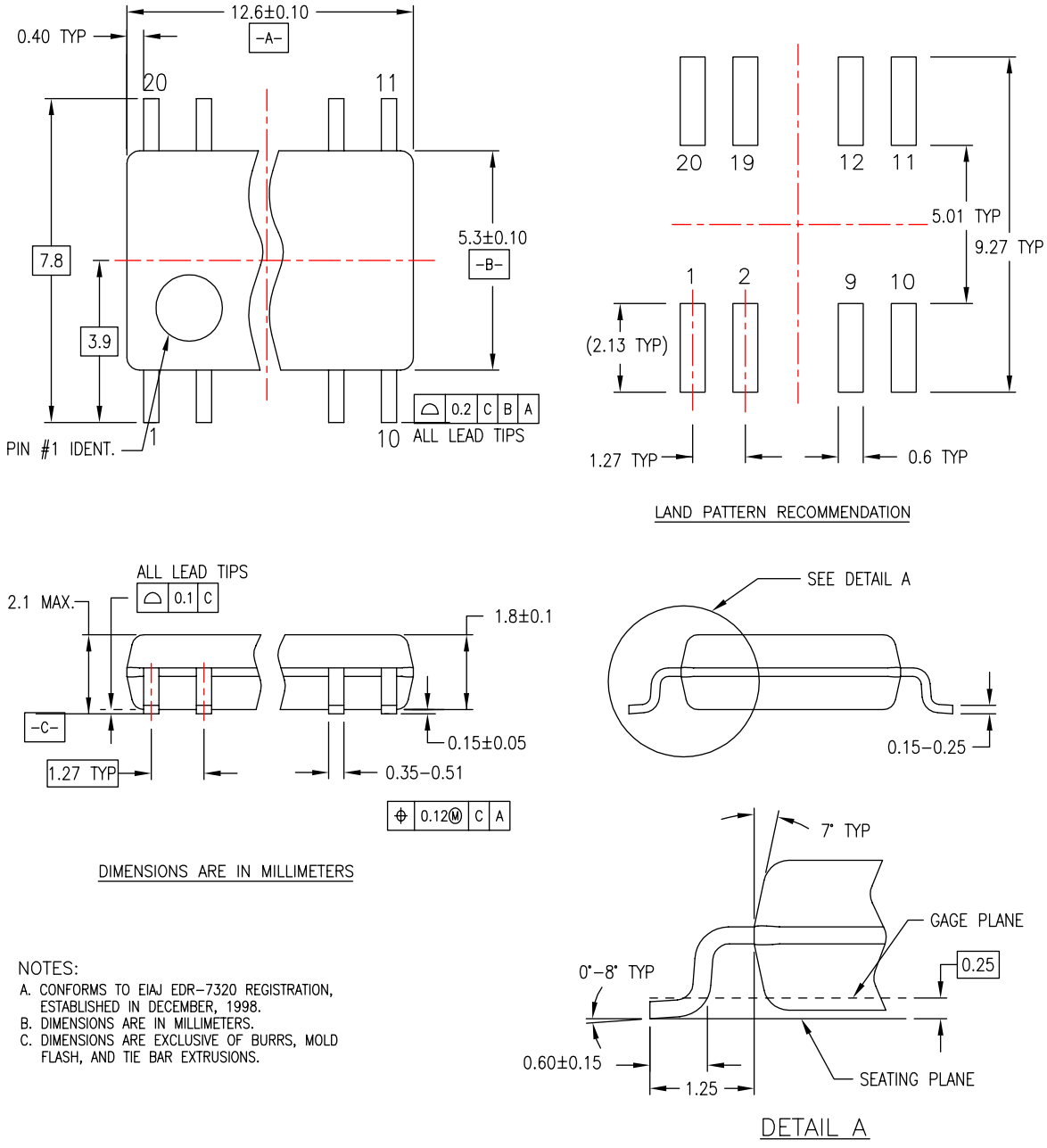
Physical Dimensions (Continued)



NOTES:

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M20DREVC

Figure 4. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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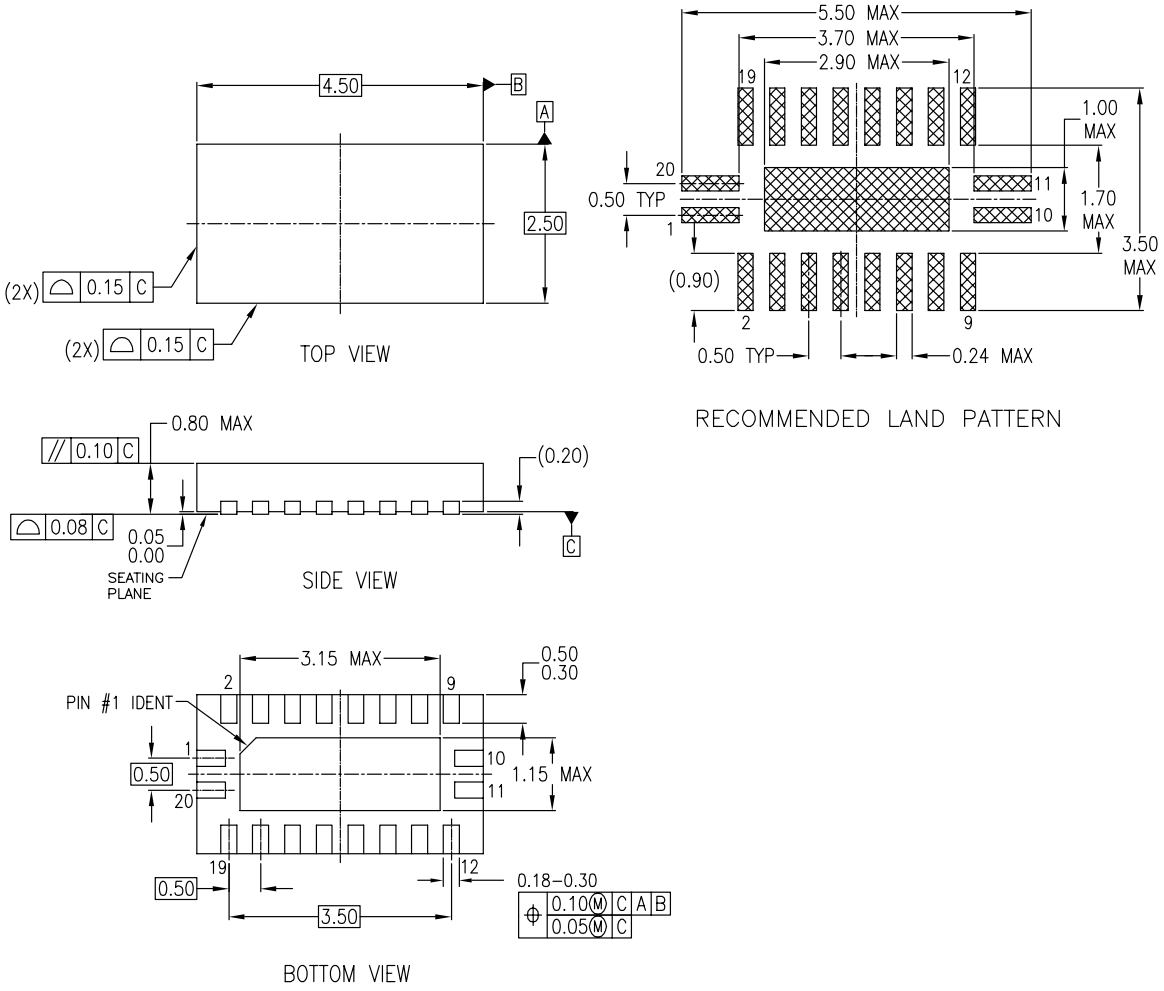
Physical Dimensions (Continued)



NOTES:

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B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP20BrevA

Figure 5. 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm

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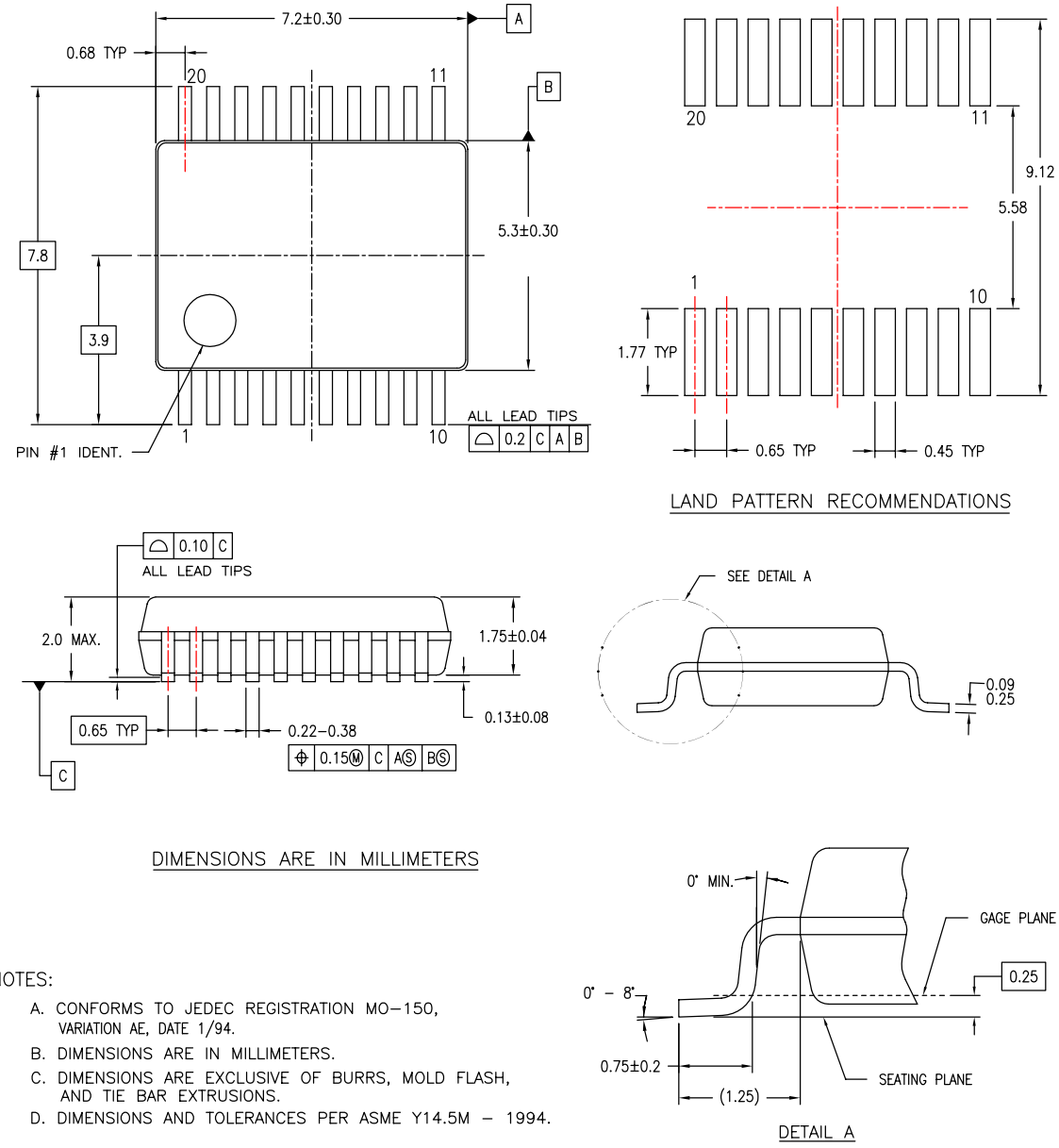

NOTES:

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D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M – 1994.

MSA20REVB

Figure 6. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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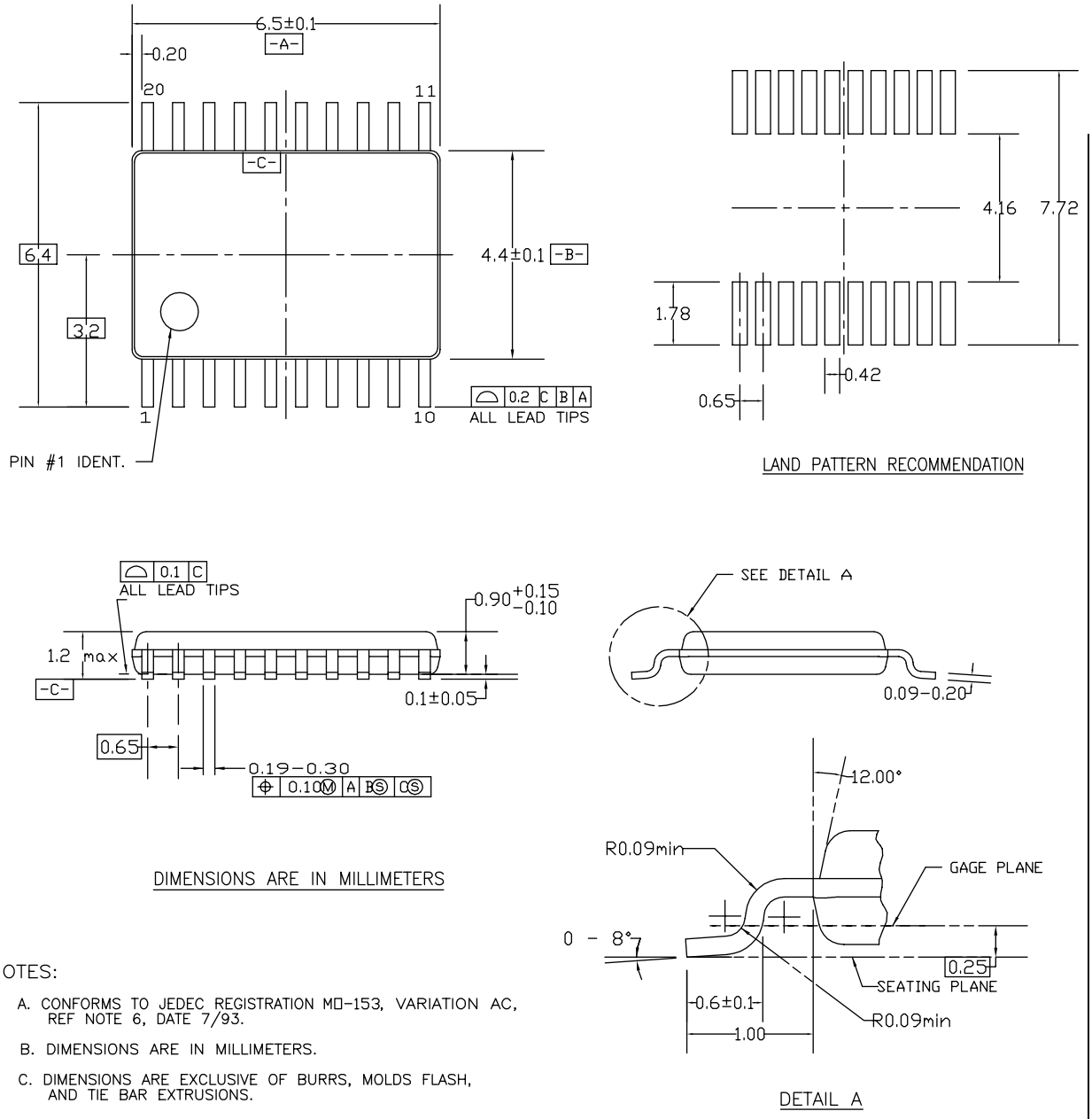
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

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D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 8. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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