8V – 60V_{IN}, 10V – 50V_{OUT}, 50 – 140W ZVS Buck-Boost Regulator

Product Description

The PI3740-00 is a high-efficiency, wide input and output range DC-DC ZVS Buck-Boost Regulator. This high-density System-in-Package (SiP) integrates controller, power switches, and support components. The integration of a high-performance Zero-Voltage Switching (ZVS) topology within the PI3740-00 increases point-of-load performance, providing best-in-class power efficiency.

The PI3740-00 requires an external inductor, resistive divider and minimal capacitors to form a complete DC-DC switching mode buck-boost regulator.

Device	Output Voltage	
	Set	Range
PI3740-00	12V	10 – 50V

The ZVS architecture also enables high-frequency operation while minimizing switching losses and maximizing efficiency. The high switching frequency operation reduces the size of the external filtering components, improves power density and enables fast dynamic response to line and load transients.

Features & Benefits

- Up to 96% efficiency
- 50 – 140W continuous output power
- Parallel-capable with single-wire current sharing
- External frequency synchronization / interleaving
- High-side current sense amplifier
- General-purpose amplifier
- Lighting / constant current mode (LGH)
- Input over / undervoltage lockout (OVLO / UVLO)
- Output overvoltage protection (OVP)
- Overtemperature protection (OTP)
- Fast and slow current limits
- –40 to 115°C operating range (T_J), -LGIZ
- –55 to 115°C operating range (T_J), -LGMZ
- Excellent light-load efficiency

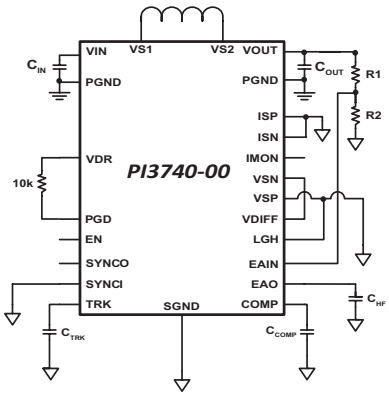
Applications

- Battery Charging and Conditioning, Telecom, Networking, Lighting
- Computing, Communications, Industrial, Automotive Accessories
- 12, 24, 48 and 60V DC–DC Applications

Package Information

- 10 x 14 x 2.56mm LGA SiP

Typical Application



PI3740-00 Modulator Gain / Output Resistance T_{PCB} = 25°C (Cont.)

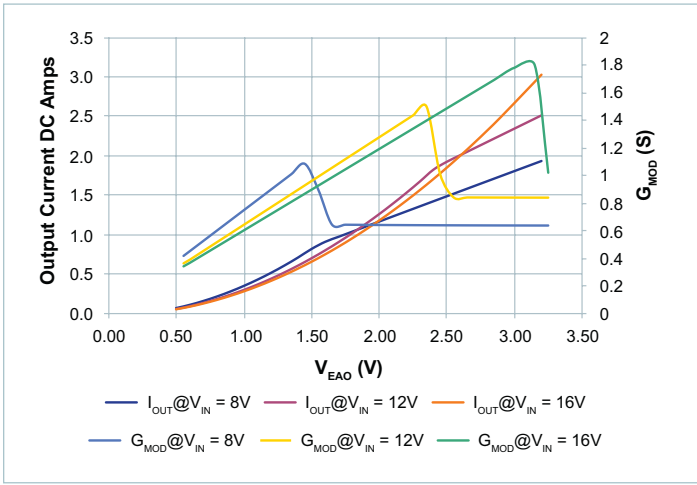


Figure 99 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 50V; 8 – 16V_{IN}*

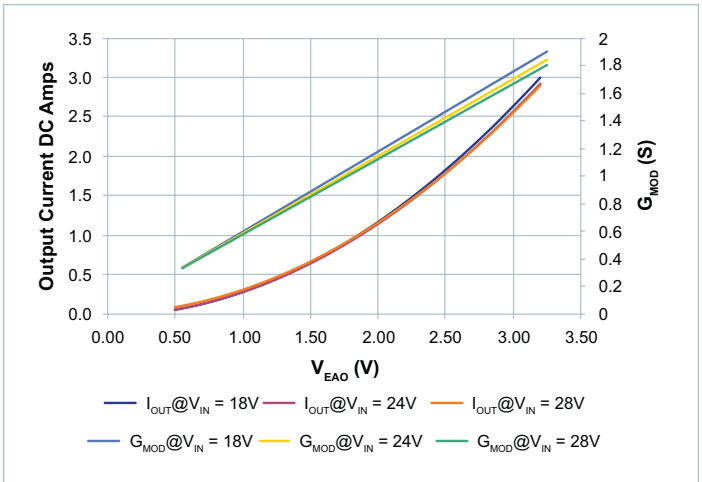


Figure 100 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 50V; 18 – 28V_{IN}*

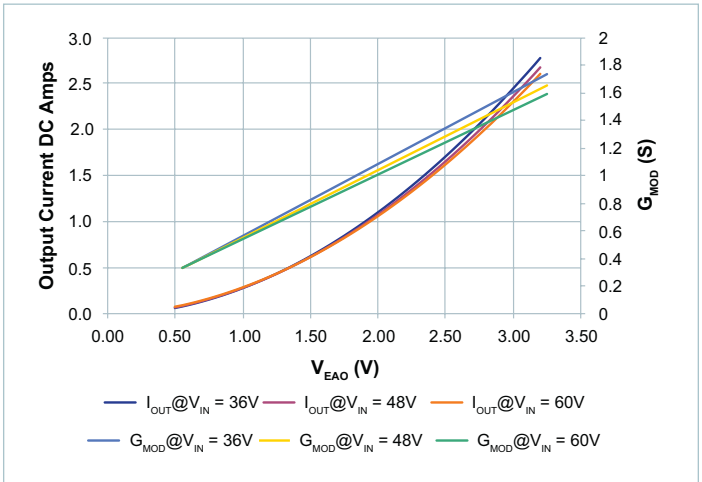


Figure 101 — *G_{MOD} vs output current vs. V_{EAO}, V_{OUT} = 50V; 36 – 60V_{IN}*

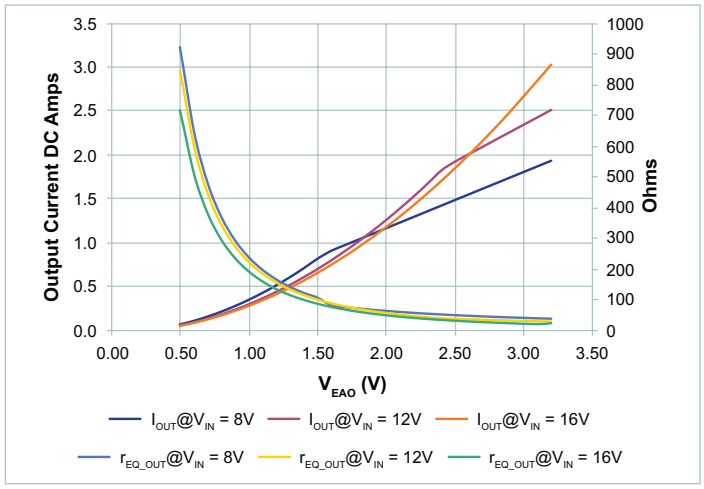


Figure 102 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 50V; 8 – 16V_{IN}*

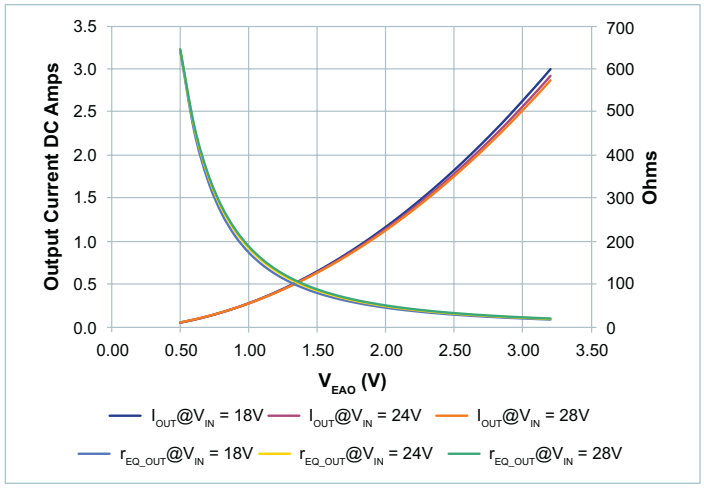


Figure 103 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 50V; 18 – 28V_{IN}*

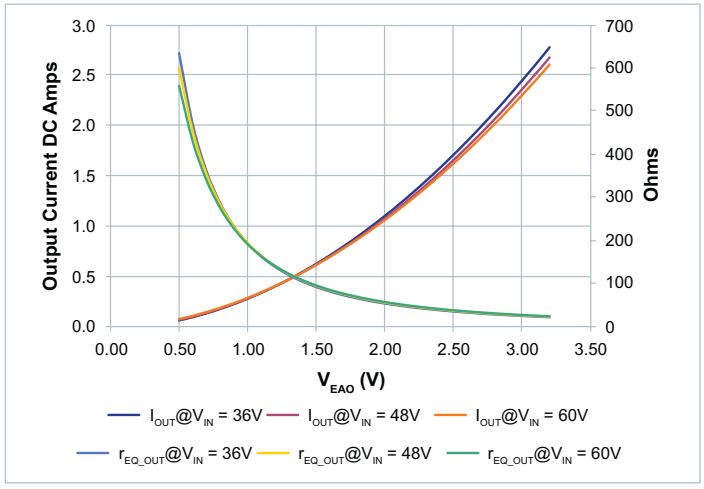


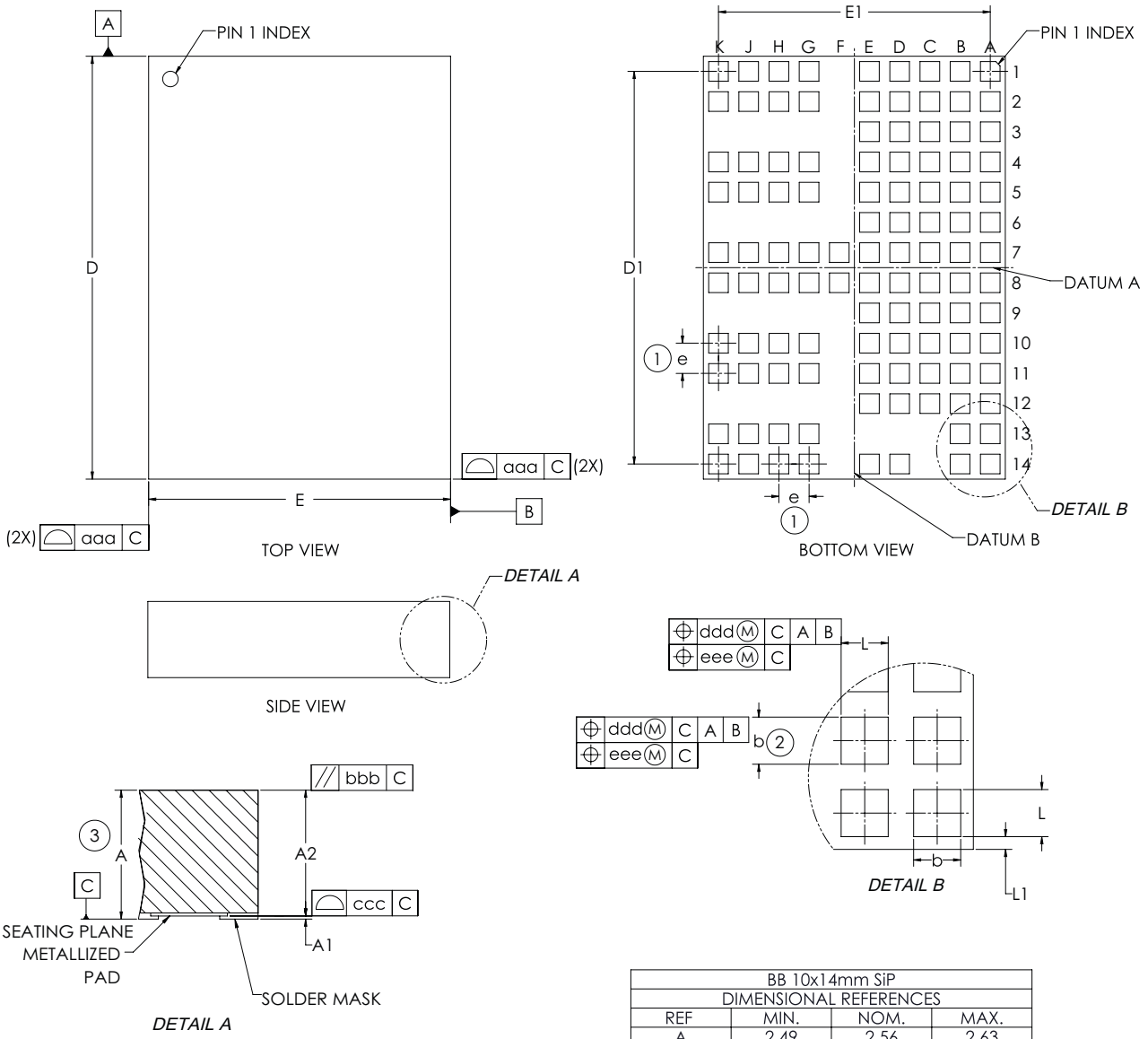
Figure 104 — *r_{EQ_OUT} vs. output current vs. V_{EAO}, V_{OUT} = 50V; 36 – 60V_{IN}*

System Design Considerations

Inductive Loads: As with all power electronic applications, consideration must be given to driving inductive loads that may be exposed to a fault in the system which could result in consequences beyond the scope of the power supply primary protection mechanisms. An inductive load could be a filter, fan motor or even excessively long cables. Consider an instantaneous short circuit through an un-damped inductance that occurs when the output capacitors are already at an initial condition of fully charged. The only thing that limits the current is the inductance of the short circuit and any series resistance. Even if the power supply is off at the time of the short circuit, the current could ramp up in the external inductor and store considerable energy. The release of this energy will result in considerable ringing, with the possibility of ringing nodes connected to the output voltage below ground. The system designer should plan for this by considering the use of other external circuit protection such as load switches, fuses, and transient voltage protectors. The inductive filters should be critically damped to avoid excessive ringing or damaging voltages. Adding a high current Schottky diode from the output voltage to PGND close to the PI3740-00 is recommended for these applications.

Low Voltage Operation: There is no isolation from an SELV (Safety-Extra-Low-Voltage) power system. Powering low voltage loads from input voltages as high as 60V may require additional consideration to protect low voltage circuits from excessive voltage in the event of a short circuit from input to output. A fast TVS (transient voltage suppressor) gating an external load switch is an example of such protection.

LGA Package Drawings

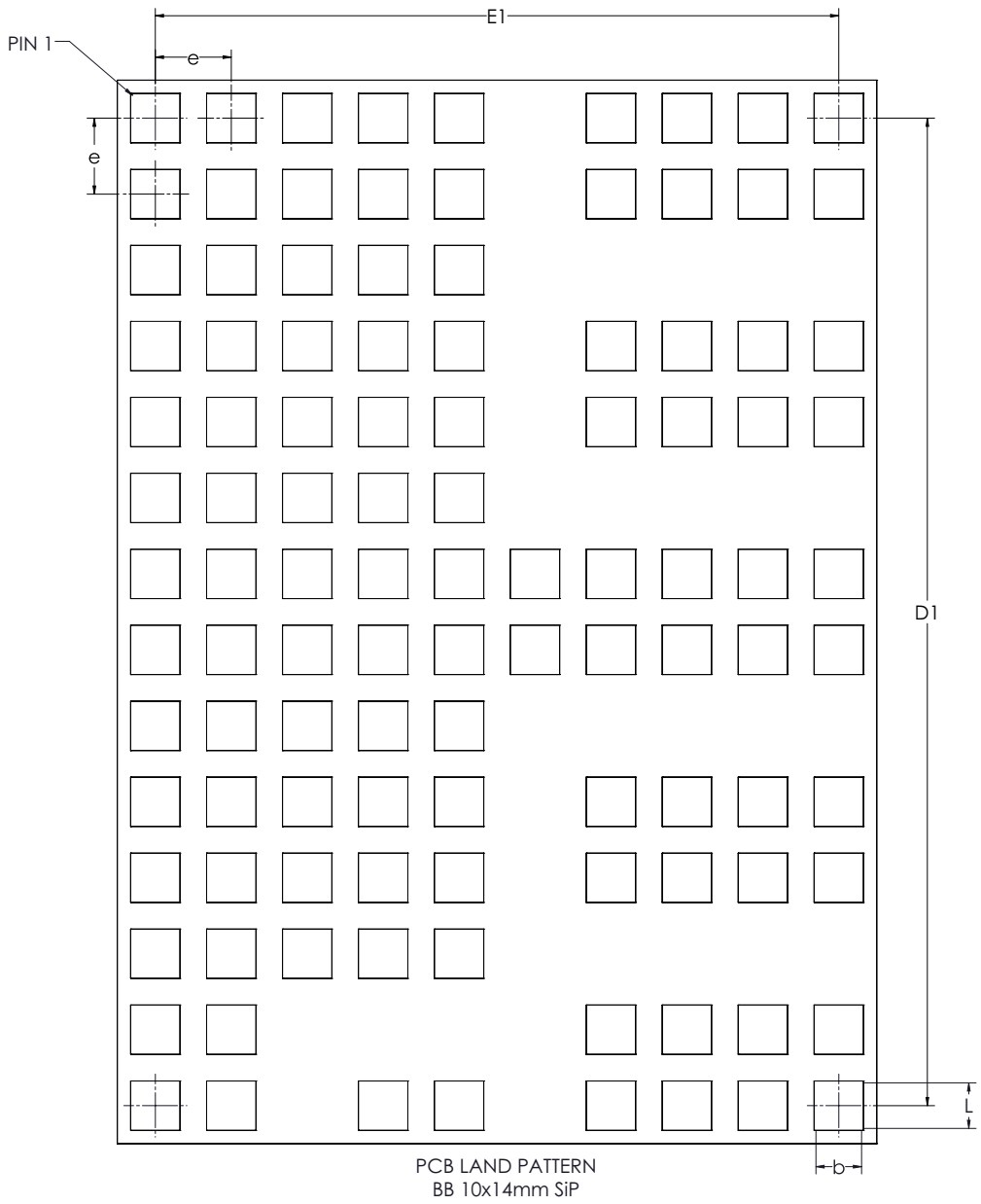


BB 10x14mm SiP	
DIMENSIONAL REFERENCES	
REF.	TOLERANCE OF FORM AND POSITION
aaa	0.10
bbb	0.10
ccc	0.08
ddd	0.10
eee	0.08

BB 10x14mm SiP			
DIMENSIONAL REFERENCES			
REF	MIN.	NOM.	MAX.
A	2.49	2.56	2.63
A1	--	--	0.04
A2	--	--	2.59
b	0.50	0.55	0.60
L	0.50	0.55	0.60
D	14.00 BSC		
E	10.00 BSC		
D1	13.00 BSC		
E1	9.00 BSC		
e	1.00 BSC		
L1	.175	0.225	.275

NOTES:
1. 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE GEOMETRIC POSITION OF THE TERMINAL AXIS.
2. DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.
3. DIMENSION 'A' INCLUDES PACKAGE WARPAGE.
4. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.
5. ALL DIMENSIONS ARE IN MM UNLESS OTHERWISE SPECIFIED.
6. RoHS COMPLIANT PER CST-0001LATEST REVISION.

LGA Receiving PCB Pattern Design Recommendations



DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
b	0.50	0.55	0.60
D1	13.00 BSC		
E1	9.00 BSC		
e	1.00 BSC		
L	0.50	0.55	0.60

Recommended receiving footprint for PI3740-00 10 x 14mm package. All pads should have a final copper size of 0.55 x 0.55mm, whether they are solder-mask defined or copper defined, on a 1 x 1mm grid. All stencil openings are 0.45mm when using either a 5 or 6mil stencil.

Revision History

Revision	Date	Description	Page Number(s)
1.0	02/10/17	Initial Release	n/a
1.1	02/27/17	Current Sense Amplifier clarifications	8
1.2	03/10/17	Miscellaneous typo corrections	7
1.3	03/31/17	Correct LGH pin name Include additional PCB Pattern information	5 46
1.4	04/27/17	Correct Absolute Min rating for V_{IN}	3
1.5	06/05/17	Update IMON Output voltage specification	8
1.6	06/16/17	Add Maximum C_{OUT} Capability at Startup section Correct Percentage of SiP Loss to Total Loss $50V_{OUT}$ figure Parallel Operation update	26 32 34
1.7	08/12/17	Update diagrams to show signal ground	1, 20, 35 – 37
1.8	08/24/17	Updated thermal impedance tables and thermal design inductor	28 – 30
1.9	06/15/18	Updated LGA package drawings Added BGA package information	46, 47 48, 49
2.0	10/12/18	Updated UVLO threshold rising min, OVLO hysteresis, overvoltage threshold, current sense amplifier IMON output at no load and transconductance error amplifier reference min/max	7, 8, 9
2.1	11/05/18	Updated V_{IN} OVLO threshold rising max spec	7
2.2	11/19/18	Updated V_{OUT} overvoltage threshold min spec	7
2.3	02/04/20	Added extended-temperature and lead solder ball options	1, 3, 6 – 10
2.4	05/15/20	Updated to add recommended Pulse Electronics inductor	22
2.5	08/12/20	Updated terminology	22
2.6	02/22/21	Updated to include PI3040-00-LGMZ part number	1, 3, 6, 7, 8, 9, 10
2.7	05/06/21	Removed BGA package option	1, 2, 3, 6, 7– 10
2.8	10/04/21	Revised inductor pairing information	22
2.9	03/11/24	Corrected note/page references	7, 8, 9, 10

Please note: Pages added in Rev 1.6 and 1.9; pages removed in Rev 2.7.

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