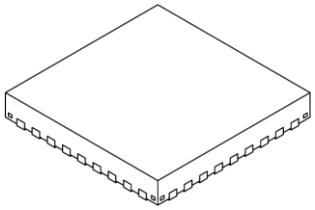
CDMOS Linear Integrated Circuit Silicon Monolithic

TC78B011FTG

Sensorless Sine-wave PWM predriver for 3-phase brushless motor

1. Outline

The TC78B011FTG is a 3-phase PWM chopper predriver for sensorless brushless motor. Motor speed can be controlled by selecting among the PWM duty cycle, analog voltage, and I²C. Non-volatile memory (NVM) is implemented and it can set according to the motors and directions for use. It also realizes closed loop speed control function without an external microcontroller. TC78B011FTG is used with six external MOSFETs inverter to drive sensorless brushless motors of which output range is wide.



P-WQFN36-0505-0.50-001

Weight: 0.06 g (typ.)

2. Applications

Fan, Pump, Portable Vacuum motors

3. Features

- Sine-wave drive
- Sensorless PWM drive
- Capable to drive Delta or Wye configured motors
- Operating voltage: 5.5 to 27V (absolute maximum rating: 30V)
- Predriver for high side and low side N-ch MOSFETs drive
- 8 selectable levels of gate drive current
- Built-in closed loop speed control with adjustable speed curve
- Motor speed control by analog voltage, PWM duty cycle, or I²C
- Serial interface (I²C) for various settings
- Standby mode (by STBY pin)
- Current monitor output (PHBF pin)
- CW/CCW control (CWCCW pin)
- Brake input pin (BRAKE pin)
- Rotation speed output (FG pin)
- Abnormality detection output (ALERT pin)
- Thermal shutdown (TSD)
- Under voltage lockout (UVLO)
- Charge pump low voltage detection (CPVSD)
- Output current limit (OCP)
- Over current detection (ISD)
- Lock protection
- Small QFN36 package

Start of commercial production
2022-01

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8.1.11. Rotation Direction

The rotation direction is determined by CWCCW pin and register setting.

Table 8.23 Rotation direction setting

Register setting 14[6] DIR	Register setting state	CWCCW pin	Direction
0	Polarity reversal disable	Low	CW
		High	CCW
1	Polarity reversal enable	Low	CCW
		High	CW

8.1.12. Brake Function

The short brake mode can be set by BRAKE pin and register setting.

Table 8.24 Brake function

BRAKE pin	Register setting 18[4] BRK_INV	Register setting description	State
Low	1	Polarity reversal enable (Low Active)	Short brake mode
	0	Polarity reversal disable (High Active)	—
High	1	Polarity reversal enable (Low Active)	—
	0	Polarity reversal disable (High Active)	Short brake mode

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8.1.13. PWM Frequency

The output PWM frequency of output is generated by dividing the IC internal clock.

Table 8.25 Output PWM frequency corresponding to dividing

Dividing	Output PWM frequency
512	23.4 kHz
256	46.9 kHz
128	93.7 kHz
64	187.5 kHz

Table 8.26 Output PWM frequency setting

Register setting 22[4:2] FPWM		Rotation speed (electrical angle)					
	Speed up	0Hz < f ≤ 200Hz	200Hz < f ≤ 400Hz	400Hz < f ≤ 600Hz	600Hz < f ≤ 800Hz	800Hz < f ≤ 1000Hz	1000Hz < f
	Speed down	0Hz < f ≤ 100Hz	100Hz < f ≤ 300Hz	300Hz < f ≤ 500Hz	500Hz < f ≤ 700Hz	700Hz < f ≤ 900Hz	900Hz < f
000	0	23.4kHz					
001	1	46.9kHz					
010	2	93.7kHz					
011	3	187.5kHz					
100	4	46.9kHz	46.9kHz	93.7kHz	93.7kHz	93.7kHz	187.5kHz
101	5	23.4kHz	46.9kHz	93.7kHz	93.7kHz	93.7kHz	93.7kHz
110	6	23.4kHz	23.4kHz	46.9kHz	46.9kHz	93.7kHz	93.7kHz
111	7	23.4kHz	46.9kHz	93.7kHz	93.7kHz	187.5kHz	187.5kHz

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8.1.14. External FET Gate Drive Output

The external FET gate drive signal is output by a drive signal generated in the IC. This product incorporates 3 half bridge predrivers, and can drive high side and low side N-ch MOSFETs. The high side of external FET gate drive voltage is VM + 8V (typ.), low side of that is 8V (typ.). Slew rate adjustment is possible with the register settings of SOURCE, and SINK.

Table 8.27 Source current setting for high side and low side FET

Register setting 23[5:3] SOURCE	Source current setting for high side and low side FET (mA)
000	10.0
001	13.9
010	19.3
011	26.8
100	37.3
101	51.8
110	72.0
111	100.0

Table 8.28 Sink current setting for high side and low side FET

Register setting 23[2:0] SINK	Sink current setting for high side and low side FET (mA)
000	20.0
001	27.8
010	38.6
011	53.7
100	74.6
101	103.6
110	143.9
111	200.0

8.1.15. Dead Time Setting

When driving the sine wave, and when the normal operation mode moves to the short brake mode with BRAKE pin and moves reverse rotation with CWCCW pin, the dead time can be set not to flow rush current to external FETs.

Table 8.29 Auto dead time control enable / disable setting

Register setting 18[0] ANTITHROUGH	Auto Dead time control
0	Enable
1	Disable

Table 8.30 Dead time setting

Register setting 22[1:0] DEADTIME	Dead time
00	250ns (3clk)
01	500ns (6clk)
10	1000ns (12clk)
11	1500ns (18clk)

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8.1.16. Speed Control Command

The speed control command is a signal which can control start, stop, and rotation count of the motor.
The type of signal is determined by SEL pin and register setting, and it can be selected among I²C, PWM duty signal, and analog voltage signal.
In case of PWM Duty signal and analog voltage signal, it is controlled by SPD pin. The polarity of the signal can be set by the register setting.

Table 8.31 Positive / negative logic process

SEL pin	Register setting 15[4] TSPSEL	Register setting 15[3] SPDINV	Speed control command	Signal polarity	State
High	—	—	I²C	—	Register setting: 27[7:0], 28[7:6] SPD [9:0] 512 to 1023 = 100%
Low	0	1	Analog voltage	Negative logic	$V_{VSP(L)}$ -> SPD command = 512 (100%) $V_{VSP(H)}$ -> SPD command =0 (0%)
		0	Analog voltage	Positive logic	$V_{VSP(L)}$ -> SPD command =0 (0%) $V_{VSP(H)}$ -> SPD command = 512 (100%)
	1	1	PWM Duty	Negative logic	Low active
		0	PWM Duty	Positive logic	High active

When the SPD signal is an analog voltage signal, the resolution is 9 bit to the voltage between $V_{VSP(L)}$ and $V_{VSP(H)}$. When the SPD signal is PWM Duty signal, the frequency range of input signal is 1 kHz to 100kHz. The Duty signal frequency is in the range of 1 kHz to 20 kHz. The resolution is 9 bit. When the frequency is 20 kHz or more, the resolution is lowered. For example, in case of 40 kHz, the resolution is 8 bit, and in case of 100 kHz, that is 7 bit.

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8.1.16.1. Speed Control Command PWM Duty

In case of positive logic, Duty is updated at a rising edge of SPD.
In case of negative logic, the polarity of the input signal is reversed in the IC. After that, the reversed signal is used as the positive logic.

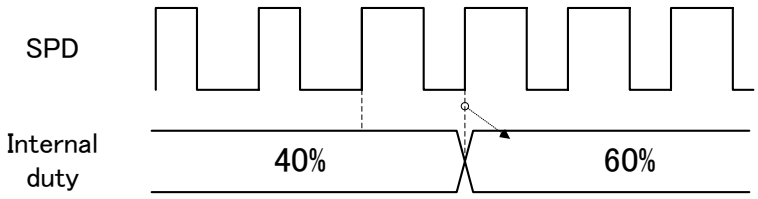

Figure 8.6 Duty update at rising edge

・When ”H” is held for 1.5ms or more from the last rising edge, the Duty is judged as 100%.

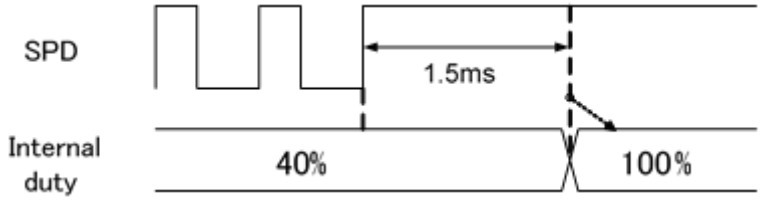

Figure 8.7 When “H” is held for 1.5ms or more from the last rising edge

・When next rising edge does not come for 100ms or more from the last rising edge, the Duty is judged as 0%.

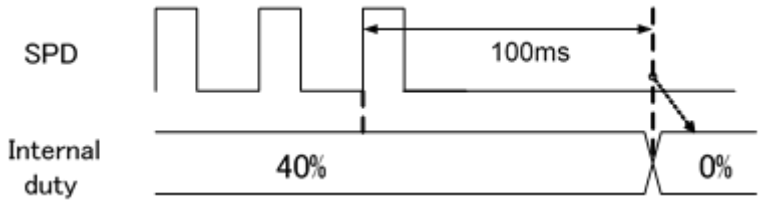

Figure 8.8 When next rising edge does not come for 100ms or more from the last rising edge

・In case of Duty=100%, a pseudo edge is generated for every 1.5ms in the IC.

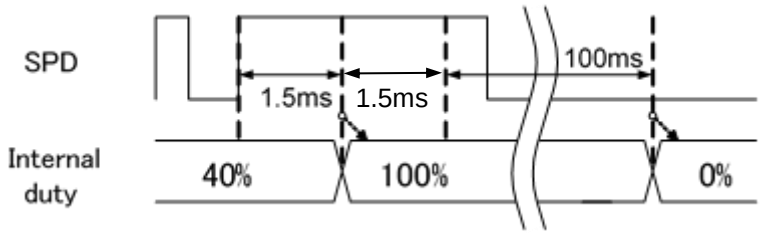

Figure 8.9 In case of Duty=100%

・ Since the maximum resolution is 9 bit to the PWM Duty input, the narrow pulses are rounded up.

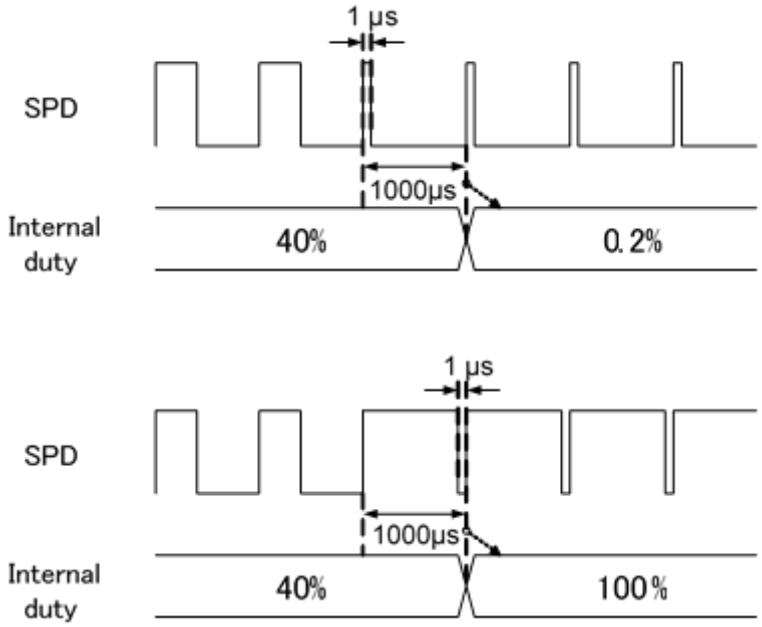

Figure 8.10 In case of rounding up the narrow pulse

8.1.17. Rotation Count Signal

The rotation count is determined by the signal which detects the motor position. It is also measured by pulse count of FG pin, or reading a value of I²C register.
FG pin is an open drain output. Register can set the pulse count outputted per rotation of the motor.
Additionally, the settings are possible that the FG signal stops according to the stop of the speed control command, and outputs while idling of the motor.

Table 8.32 Relational equation between register setting value and rotation frequency

Register setting 29[7:0] 30[7:0]	Relational equation of rotation frequency per 1 electrical angle
hz_cnt[15:0]	Rotation frequency[Hz]=250000/hz_cnt[15:0]

Table 8.33 FG setting and output pulse per rotation of motor

Register setting 15[7:5] FGSEL	FG signal setting	Number of poles of motor				
		2 poles	4 poles	6 poles	8 poles	10 poles
000	1 ppr	1	2	3	4	5
001	Banned					
010						
011						
100						
101						
110						
111						

Table 8.34 FG signal control setting

Register setting 14[0] FG_ON	FG signal setting
0	FG stops without speed control command
1	FG outputs without speed control command

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8.1.18. Number of Poles and Rotation count of Motor

The part which is controlled by the rotation count [rpm] such as a speed control, is controlled by the number of poles (POLEPAIR) setting. It converts 1 electric angle frequency to the rotation count [rpm], and is controlled.

Rotation count [rpm] = 1 electric angle frequency × (60s/ (Number of poles/2))

Table 8.35 Number of pole of motor

Register setting 14[5:3] POLEPAIR	Number of poles of motor
000	2
001	4
010	6
011	8
100	10
101	12
110	14
111	16

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8.2. Speed control

The speed control of motors can be selected from Closed loop control and Open loop control.

Table 8.36 Speed control setting

Register setting 11[0] OPENLOOP	Speed control
0	Closed loop
1	Open loop

8.2.1. Closed loop Control

The basic speed curve (relation between SPD signal value and rotation speed) of Closed loop speed control is as follows;

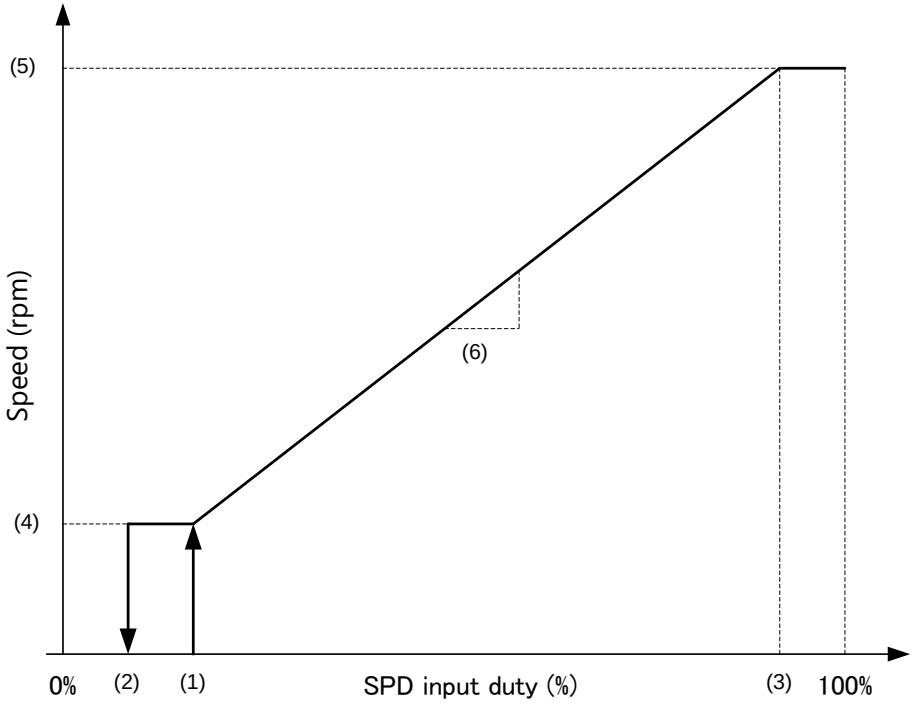

Figure 8.11 Speed curve example in Closed loop speed control

Table 8.37 List of Closed loop setting

Description	Setting range	Setting method	Resolution
(1) Start Duty	0 to 49.8%	STARTDUTY / 512	0.2%
(2) Stop Duty	0 to 49.6%	STOPDUTY × 2 / 512	0.4%
(3) Max Duty	50.2 to 100%	(MAXDUTY + 257) / 512	0.2%
(4) Start rotation count (Start RPM)	0 to 4095	STARTRPM	1rpm
(5) Max rotation count (Max RPM)	Depending on (1), (3), and (6)	N/A	N/A
(6) Speed Slope	0 to 1280 rpm/%	SPEEDSLOP × 0.08	0.08rpm/%

The maximum resolution is 9 bit for the SPD signal.

- When the SPD signal is an analog voltage signal, the resolution is 9 bit to the voltage between $V_{VSP(L)}$ and $V_{VSP(H)}$.
- In the PWM Duty input, when the frequency of Duty signal is in the range of 1 kHz to 20 kHz, the resolution is 9 bit. When the frequency is 20 kHz or more, the resolution is lowered. For example, in case of 40 kHz, the resolution is 8 bit, and in case of 100 kHz, that is 7 bit.

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Example of parameter setting:
Setting target:
Start Duty=20%, Stop Duty=18%, Max Duty=90%
Start RPM=1500rpm, Max RPM=15000rpm

Table 8.38 Example of parameter setting

Register address	Register name	Setting range	Equation	Calculation example
3[7:0]	STARTDUTY [7:0]	0 to 255 (0% to 49.8%)	Start Duty × 512	0.20 × 512 =102
2[6:0]	STOPDUTY [6:0]	0 to 127 (0% to 49.6%)	Stop Duty × 256	0.18 × 256 = 46
5[7:0]	MAXDUTY[7:0]	0 to 255 (50.2% to 100%)	Max Duty × 512 – 257	0.90 × 512 – 257 = 204
6[7:0] 7[7:4]	STARTRPM[11:0]	0 to 4095 (0rpm to 4095rpm)	Start rotation count	1500
8[7:0] 9[7:2]	SPEEDSLOP [13:0]	0 to 16383 (0rpm/% to 1280rpm/%)	64×(Max RPM – Start RPM) / (MAXDUTY –STARTDUTY + 257)	(15000 – 1500) / (204 – 102 + 257) × 64=2407

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Option (1): Max Duty or more Closed loop-> Open loop (Output Duty= Input Duty)
If it is enabled, MAXOPEN should be set to 1.
The hysteresis to the change Duty can be set in MAXDUTYHYS.

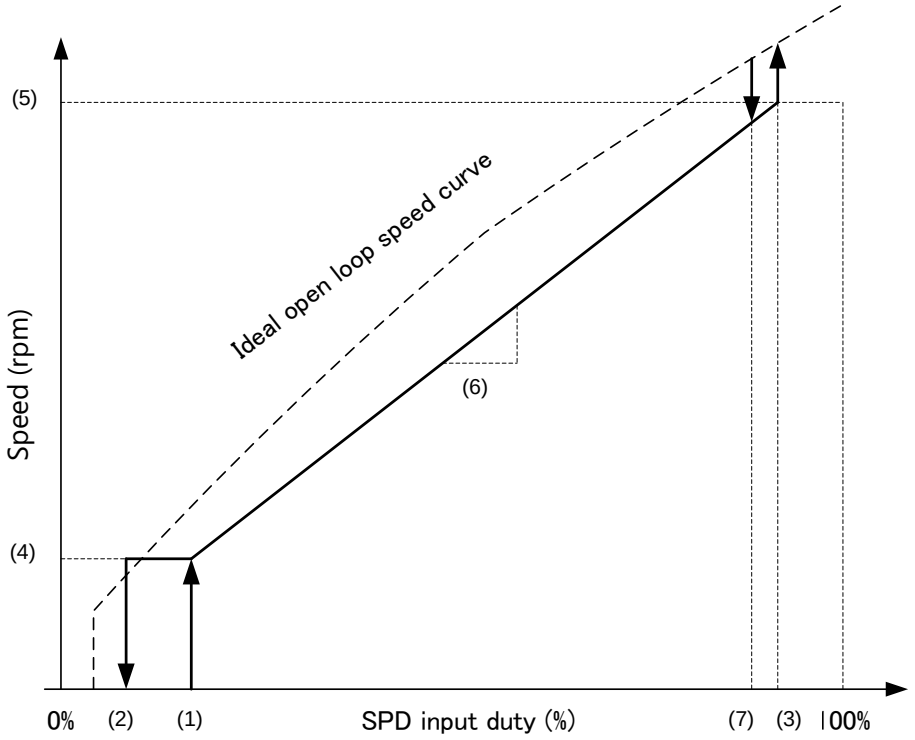

Figure 8.12 Example of Closed loop speed curve (option (1))

Table 8.39 Closed loop setting of option (1)

Description	Setting range	Setting method	Resolution
(1) Start Duty	0 to 49.8%	STARTDUTY / 512	0.2%
(2) Stop Duty	0 to 49.6%	STOPDUTY × 2 / 512	0.4%
(3) Max Duty Closed loop to Open loop	50.2 to 100%	(MAXDUTY + 257) / 512	0.2%
(4) Start rotation count (Start RPM)	0 to 4095	STARTRPM	1rpm
(5) Max rotation count (Max RPM)	Depending on (1), (3), and (6)	N/A	N/A
(6) Speed Slope	0 to 1280 rpm/%	SPEEDSLOP × 0.08	0.08rpm/%
(7) Open loop to Closed loop	(Max Duty – 6.4%) to (Max Duty – 0.4%)	(MAXDUTY + 257 - (MAXDUTYHYS + 1) × 2) / 512	0.4%

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Example of parameter setting:
Setting target:
Start duty=20%, Stop duty=18%, Max duty=90%, Max duty hysteresis=4%(86%)
Start RPM=1500 rpm, Max RPM=15000 rpm

Table 8.40 Example of Closed loop parameter setting for option (1)

Register address	Register name	Setting range	Equation	Calculation example
3[7:0]	STARTDUTY [7:0]	0 to 255 (0% to 49.8%)	Start Duty × 512	0.20 × 512 =102
2[6:0]	STOPDUTY [6:0]	0 to 127 (0% to 49.6%)	Stop Duty × 256	0.18 × 256 = 46
5[7:0]	MAXDUTY [7:0]	0 to 255 (50.2% to 100%)	Max Duty × 512 – 257	0.90 × 512 – 257 = 204
6[7:0] 7[7:4]	STARTRPM[11:0]	0 to 4095 (0rpm to 4095rpm)	Start rotation count	1500
8[7:0] 9[7:2]	SPEEDSLOP [13:0]	0 to 16383 (0rpm/% to 1280rpm/%)	64×(Max RPM – Start RPM) / (MAXDUTY –STARTDUTY + 257)	(15000-1500)/(204 – 102 + 257) × 64 = 2407
7[3:0]	MAXDUTYHYS [3:0]	0 to 15 (0.4% to 6.4%)	(Max duty hysteresis [%] / 0.4) – 1	4 / 0.4 – 1=9

Option (2): NOSTOP, MAXOFF setting
According to the setting, the operation of which SPD command is start Duty or less, is as follows.

Table 8.41 Operation of which SPD command is start Duty or less, in Closed loop control

Register setting 9[1] MAXOPEN	Register setting 2[7] NOSTOP	Register setting 9[0] MAXOFF	Target speed		
			SPD duty =0%	0% < SPD duty ≤ Stop Duty	Stop Duty < SPD duty ≤ Start duty
0	0	0	0	0	Duty up: 0 Duty down: Start rotation count
	0	1	Max rotation count	0	Duty up: 0 Duty down: Start rotation count
	1	0	Start rotation count	Start rotation count	Start rotation count
	1	1	Max rotation count	Max rotation count	Start rotation count
1	0	0	0	0	Duty up: 0 Duty down: Start rotation count
	0	1	100% Output	0	Duty up: 0 Duty down: Start rotation count
	1	0	Start rotation count	Start rotation count	Start rotation count
	1	1	100% Output	100% Output	Start rotation count

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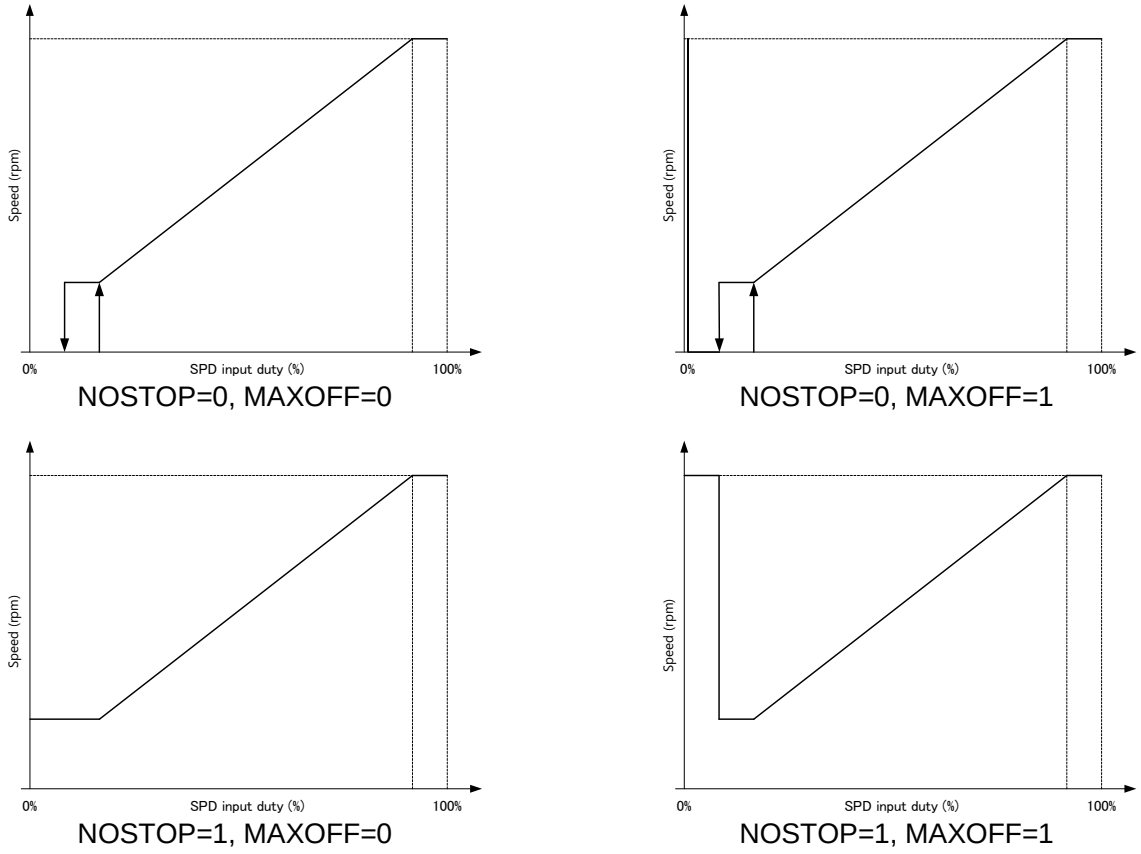

Figure 8.13 Example of Closed loop speed curve (option (2)) (MAXOPEN=0)

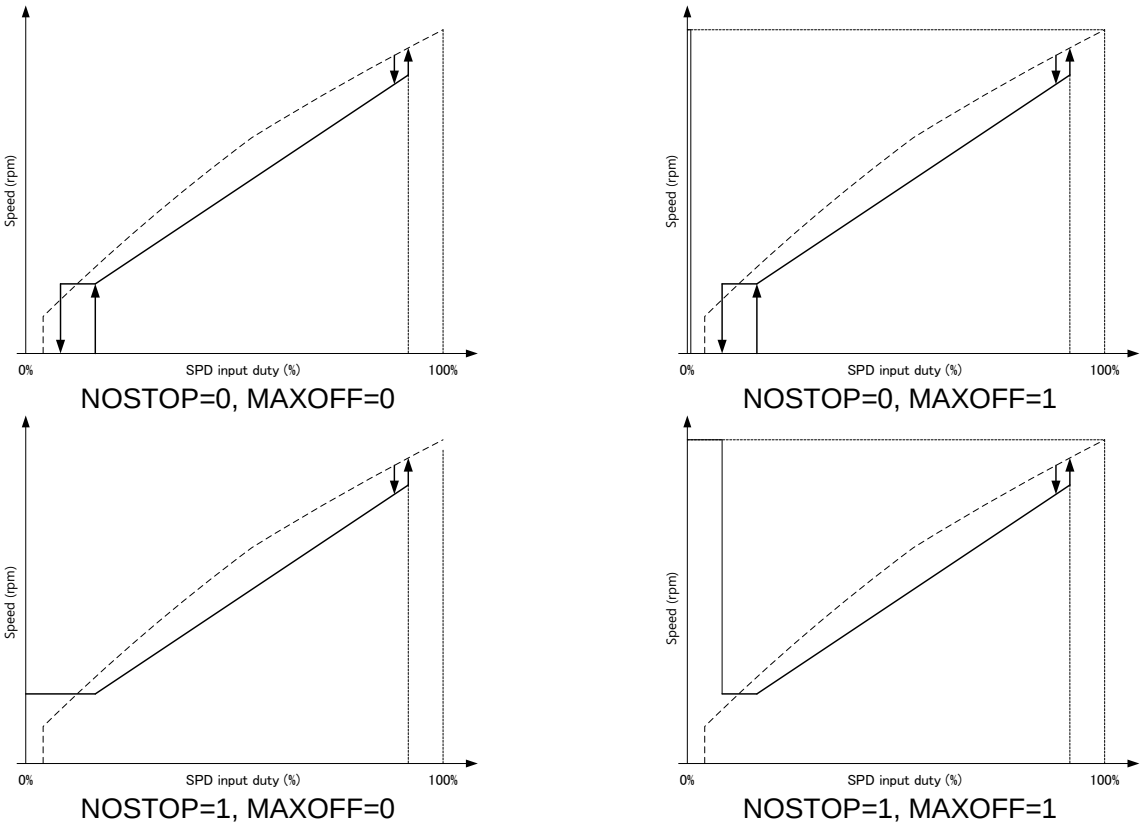

Figure 8.14 Example of Closed loop speed curve (option (2)) (MAXOPEN=1)

Option (3): Addition of change duty point

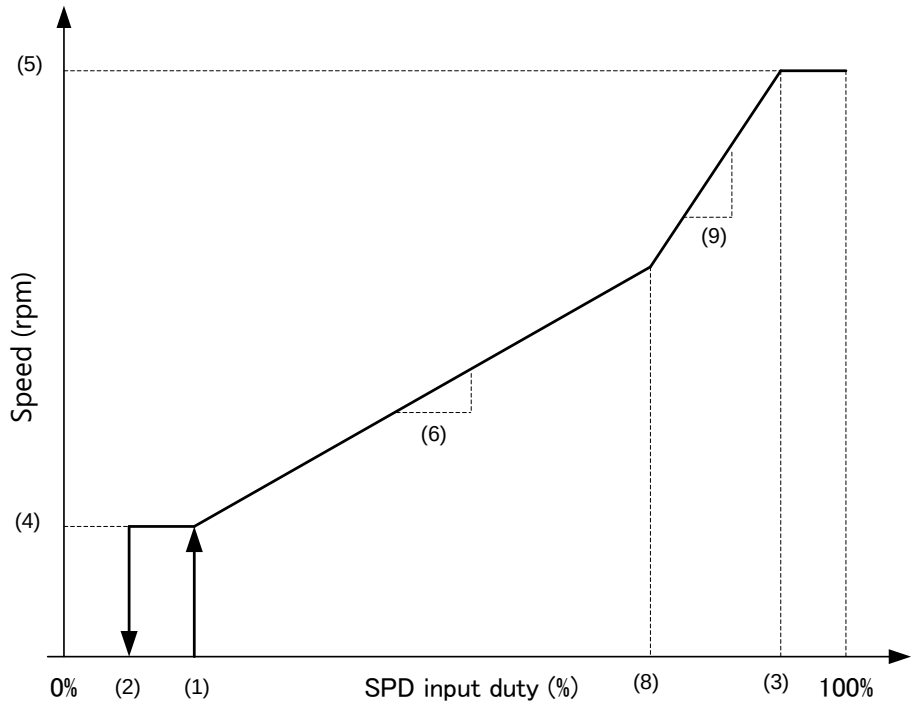

Figure 8.15 Example of Closed loop speed curve (option (3))

Table 8.42 List of Closed loop setting for option (3)

Description	Setting range	Setting method	Resolution
(1) Start Duty	0 to 49.8%	STARTDUTY / 512	0.2%
(2) Stop Duty	0 to 49.6%	STOPDUTY × 2 / 512	0.4%
(3) Max Duty	50.2 to 100%	(MAXDUTY + 257) / 512	0.2%
(4) Start rotation count (Start RPM)	0 to 4095	STARTRPM	1rpm
(5) Max rotation count (Max RPM)	Depending on (1), (3), and (6)	N/A	N/A
(6) Speed Slope 1	0 to 1280 rpm/%	SPEEDSLOP × 0.08	0.08rpm/%
(8) Change Duty	0.4 to 99.6%	CHANGEDUTY × 2 / 512	0.4%
(9) Speed Slope 2	0 to 1280 rpm/%	SPEEDSLOP2 × 0.08	0.08rpm/%

When the change Duty point is used, the change Duty should be set between start Duty and max. Duty. When the change Duty is not used, CHANGEDUTY should be set to 0.

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Example of parameter setting:
Setting target:
Start Duty=20%, Stop Duty=18%, Max Duty=90%
Start RPM=1500rpm, 50%Duty RPM=5000rpm, Max RPM=15000rpm

Table 8.43 Example of Closed loop parameter setting for option (3)

Register address	Register name	Setting range	Equation	Calculation example
3[7:0]	STARTDUTY [7:0]	0 to 255 (0% to 49.8%)	Start Duty × 512	0.20 × 512 = 102
2[6:0]	STOPDUTY [6:0]	0 to 127 (0% to 49.6%)	Stop Duty × 256	0.18 × 256 = 46
5[7:0]	MAXDUTY [7:0]	0 to 255 (50.2% to 100%)	Max Duty × 512 – 257	0.90 × 512 – 257 = 204
4[7:0]	CHANGEDUTY [7:0]	1 to 255 (0.4% to 99.6%)	Change Duty × 256	0.50 × 256 = 128
6[7:0] 7[7:4]	STARTRPM[11:0]	0 to 4095 (0rpm to 4095rpm)	Start RPM	1500
8[7:0] 9[7:2]	SPEEDSLOP [13:0]	0 to 16383 (0rpm/% to 1280rpm/%)	64×(Change Duty RPM – Start RPM) / (CHANGEDUTY × 2 – STARTDUTY)	(5000-1500) / (128×2-102) × 64 = 1455
10[7:0] 11[7:2]	SPEEDSLOP2 [13:0]	0 to 16383 (0rpm/% to 1280rpm/%)	64×(Max RPM – Change Duty RPM) / (MAXDUTY + 257 – CHANGEDUTY × 2)	(15000 - 5000) / (204 + 257 – 128 × 2) × 64 = 3122

Addition of change duty can be used with option (1) and (2).

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8.2.2. Limitation of the Rotation Count Change

By limiting the change amount in case of decreasing the rotation count, the motor avoids stopping when the rotation count of the motor is lowered rapidly.

Table 8.44 Limitation setting of the rotation count change

Register setting 18[7:5] RPMLIMIT	Rotation count change (rpm)
000	No limitation
001	512
010	2200
011	3800
100	5400
101	7000
110	8600
111	10240

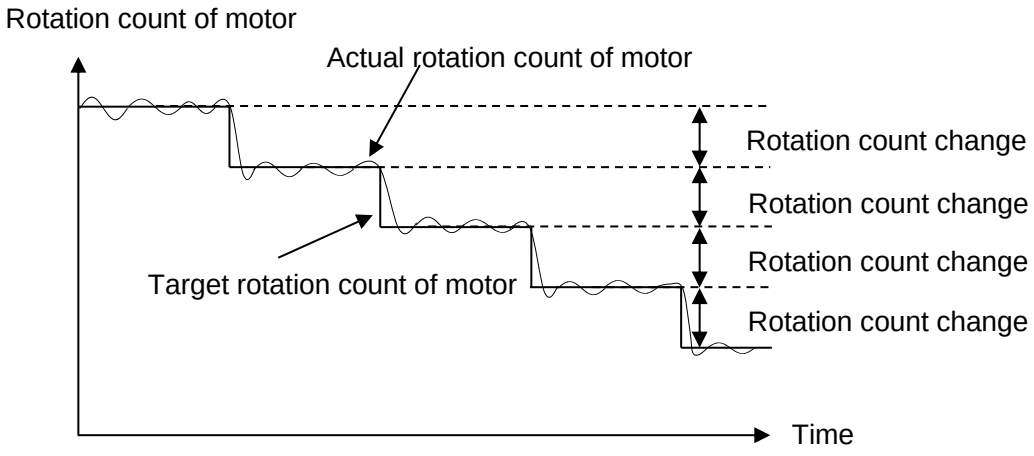

Figure 8.16 Image until actual rotation count reaches target count

8.2.3. Open Loop Speed Control

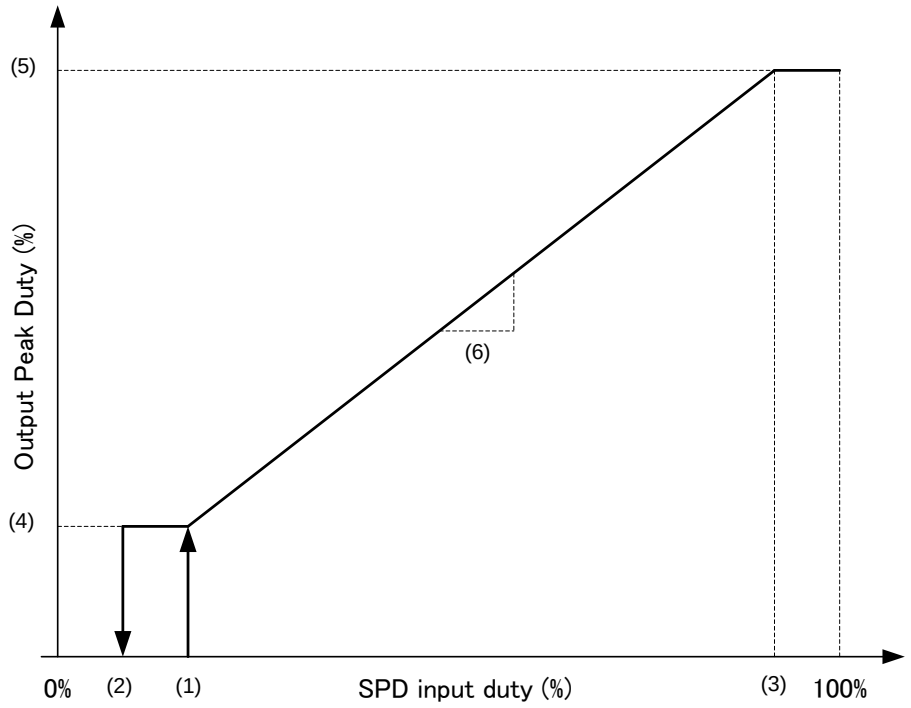

Figure 8.17 Speed curve example in Open loop speed control

Table 8.45 List of Open loop setting

Description	Setting range	Setting method	Resolution
(1) Start Duty	0 to 49.8%	STARTDUTY / 512	0.2%
(2) Stop Duty	0 to 49.6%	STOPDUTY × 2 / 512	0.4%
(3) Max Duty	50.2 to 100%	(MAXDUTY + 257) / 512	0.2%
(4) Min output	0 to 49.8%	STARTRPM[11:4] / 512	0.2%
(5) Max output	Depending on (1), (3), and (6)	N/A	N/A
(6) Speed Slope	0 to 16 output %/ input %	SPEEDSLOP / 1024	1/1024 output %/ input %

The maximum resolution is 9 bit for the SPD signal.

- When the SPD signal is an analog voltage signal, the resolution is 9 bit to the voltage between $V_{VSP(L)}$ and $V_{VSP(H)}$.
- In the PWM Duty input, when the frequency of Duty signal is in the range of 1 kHz to 20 kHz, the resolution is 9 bit. When the frequency is 20 kHz or more, the resolution is lowered. For example, in case of 40 kHz, the resolution is 8 bit, and in case of 100 kHz, that is 7 bit.

When the output PWM frequency is 23.4 kHz, the output PWM resolution is 9 bit. If the output PWM frequency is high, the output resolution is lowered.

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Example of parameter setting:
Setting target:
Start Duty=20%, Stop Duty=18%, Max Duty=90%
Min output Duty=10%, Max output Duty=95%

Table 8.46 Example of Open loop parameter setting

Register address	Register name	Setting range	Equation	Calculation example
3[7:0]	STARTDUTY [7:0]	0 to 255 (0% to 49.8%)	Start Duty × 512	0.20 × 512 =102
2[6:0]	STOPDUTY [6:0]	0 to 127 (0% to 49.6%)	Stop Duty × 256	0.18 × 256 = 46
5[7:0]	MAXDUTY[7:0]	0 to 255 (50.2% to 100%)	Max Duty × 512 – 257	0.90 × 512 – 257 = 204
6[7:0]	STARTRPM[11:4]	0 to 255 (0% to 49.8%)	Min output Duty × 512	0.10 × 512 = 51
8[7:0] 9[7:2]	SPEEDSLOP [13:0]	0 to 16383 (0 output / input % to 16 output / input %)	1024 × (Max output Duty × 512 – STARTRPM)/(MAXDUTY – STARTDUTY + 257)	(0.95 × 512 – 51)/(204 + 257 – 102) × 1024 = 1241

Option (1): Max Duty or more, Output Duty=Input Duty
If it is enabled, MAXOPEN should be set to 1.
The hysteresis to the change Duty can be set in MAXDUTYHYS.

Option (2): NOSTOP, MAXOFF setting
According to the setting, the operation of which SPD command is start Duty or less, is as follows.

According to MAXOPEN, NOSTOP, and MAXOFF settings, the operation of which Duty is start Duty or less, is as follows.

Table 8.47 List of MAXOPEN, NOSTOP, and MAXOFF settings

Register setting 9[1] MAXOPEN	Register setting 2[7] NOSTOP	Register setting 9[0] MAXOFF	Target speed		
			SPD duty =0%	0% < SPD duty ≤ Stop Duty	Stop Duty < SPD duty ≤ Start duty
0	0	0	0	0	Duty up: 0 Duty down: Min Output
	0	1	Max Output	0	Duty up: 0 Duty down: Min Output
	1	0	Min Output	Min Output	Min Output
	1	1	Max Output	Max Output	Min Output
1	0	0	0	0	Duty up: 0 Duty down: Min Output
	0	1	100% Output	0	Duty up: 0 Duty down: Min Output
	1	0	Min Output	Min Output	Min Output
	1	1	100% Output	100% Output	Min Output

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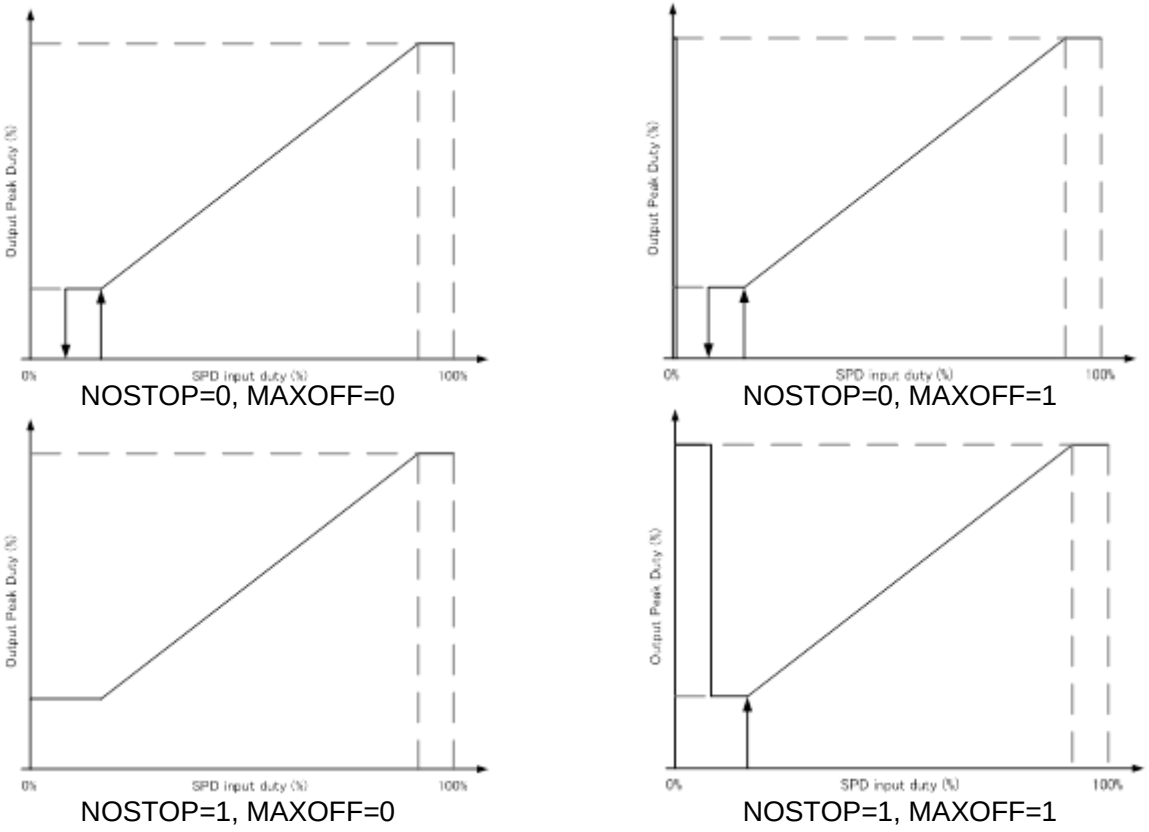

Figure 8.18 Example of Open loop speed curve (option (2)) (MAXOPEN = 0)

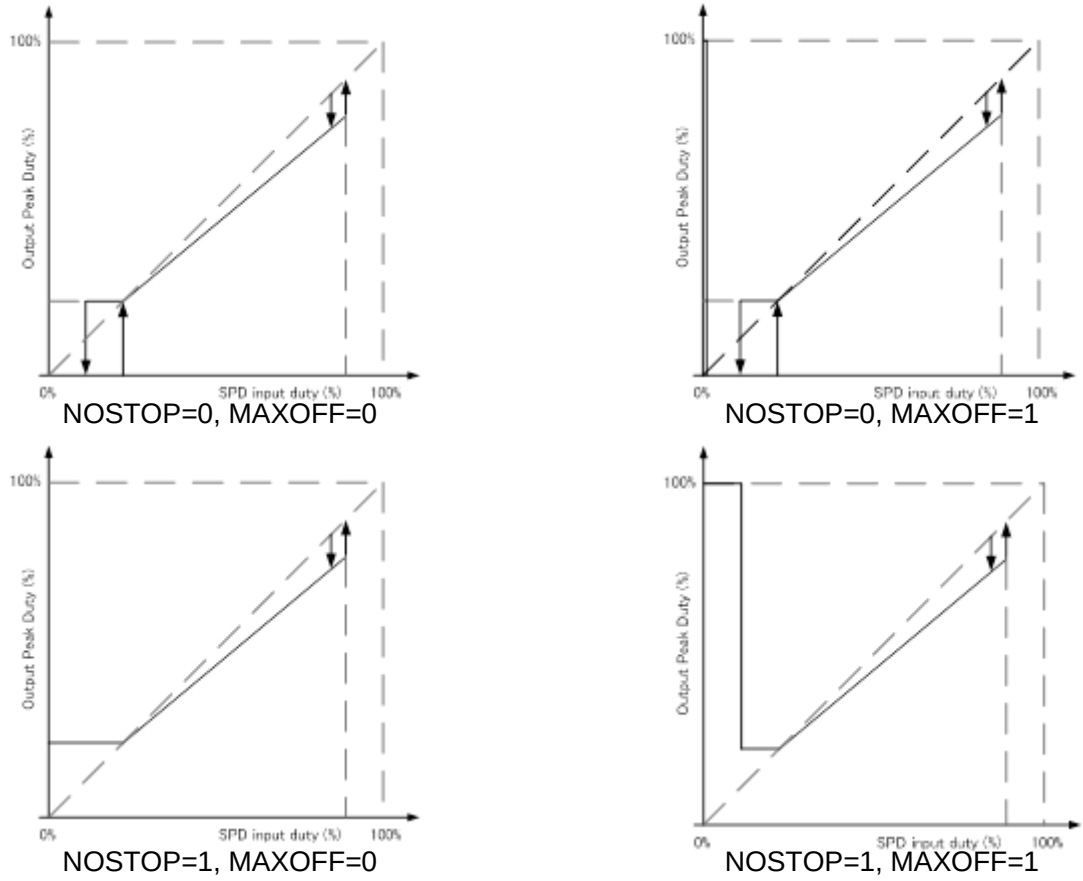

Figure 8.19 Example of Open loop speed curve (option (2)) (MAXOPEN = 1)

Option (3): Addition of change duty point

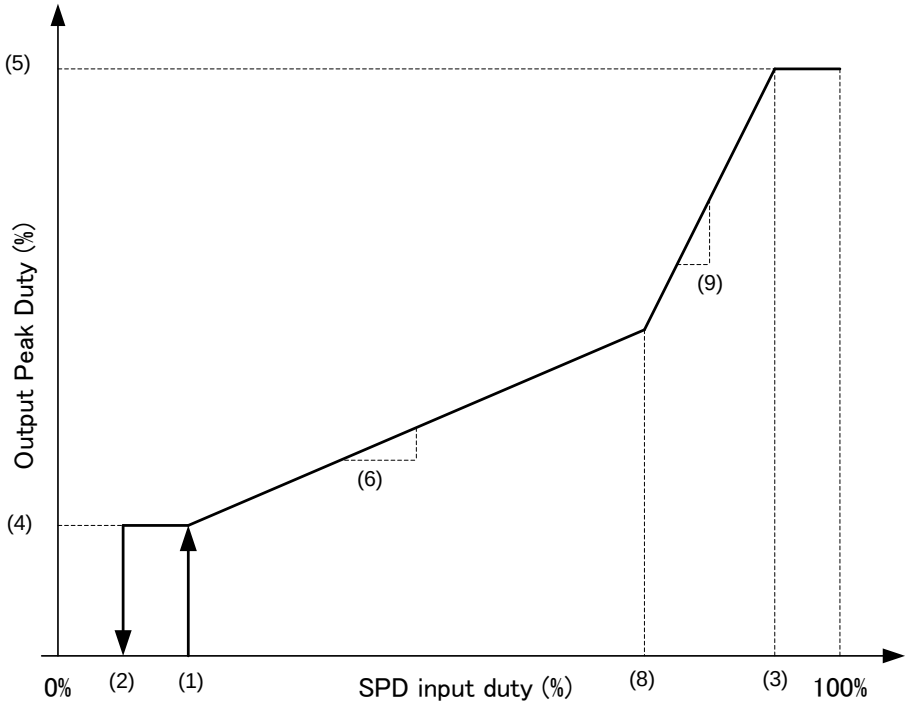

Figure 8.20 Example of Open loop speed curve (option (3))

Table 8.48 List of Open loop settings for opstion (3)

Description	Setting range	Setting method	Resolution
(1) Start Duty	0 to 49.8%	STARTDUTY / 512	0.2%
(2) Stop Duty	0 to 49.6%	STOPDUTY × 2 / 512	0.4%
(3) Max Duty	50.2 to 100%	(MAXDUTY + 257) / 512	0.2%
(4) Min output	0 to 49.8%	STARTRPM[11:4] / 512	0.2%
(5) Max output	Depending on (1), (3), and (6)	N/A	N/A
(6) Speed Slope 1	0 to 16output % / input %	SPEEDSLOP / 1024	1/1024 output %/ input %
(8) Change Duty	0.4 to 99.6%	CHANGEDUTY × 2 / 512	0.4%
(9) Speed Slope 2	0 to 16output % / input %	SPEEDSLOP2 / 1024	1/1024 output %/ input %

When the change Duty point is used, the change Duty should be set between start Duty and max. Duty. When the change Duty is not used, CHANGEDUTY should be set to 0.

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Example of parameter setting:
Setting target:
Start Duty=20%, Stop Duty=18%, Max Duty=90%, Change Duty=50%
Start output Duty =10%, Output duty at Change Duty=40%, Max output Duty=95%

Table 8.49 Example of Open loop parameter setting for option (3)

Register address	Register name	Setting range	Equation	Calculation example
3[7:0]	STARTDUTY [7:0]	0 to 255 (0% to 49.8%)	Start Duty × 512	0.20 × 512 = 102
2[6:0]	STOPDUTY [6:0]	0 to 127 (0% to 49.6%)	Stop Duty × 256	0.18 × 256 = 46
5[7:0]	MAXDUTY [7:0]	0 to 255 (50.2% to 100%)	Max Duty × 512 – 257	0.90 × 512 – 257 = 204
4[7:0]	CHANGEDUTY [7:0]	1 to 255 (0.4% to 99.6%)	Change Duty × 256	0.50 × 256 = 128
6[7:0]	STARTRPM [11:4]	0 to 255 (0% to 49.8%)	Min output Duty × 512	0.10 × 512 = 51
8[7:0] 9[7:2]	SPEEDSLOP [13:0]	0 to 16383 (0 output % / input % to 16 output % / input %)	1024 × (Output Duty at Change Duty × 512 – STARTRPM) / (CHANGEDUTY × 2 – STARTDUTY)	(0.40 × 512 – 51) / (128 × 2 – 102) × 1024 = 1022
10[7:0] 11[7:2]	SPEEDSLOP2 [13:0]	0 to 16383 (0 output %/ input % to 16 output % / input %)	1024 × (Max output Duty × 512 – Output duty at Change Duty) / (MAXDUTY – CHANGEDUTY × 2 + 257)	(0.95 × 512 – 0.40 × 512) / (204 + 257 – 128 × 2) × 1024 = 1404

Addition of change duty can be used with option (1) and (2).

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8.3. I²C and NVM

Data of internal registers can be communicated via I²C. Each setting parameter is read from non-volatile memory (NVM), and is stored to the register.

8.3.1. I²C communication

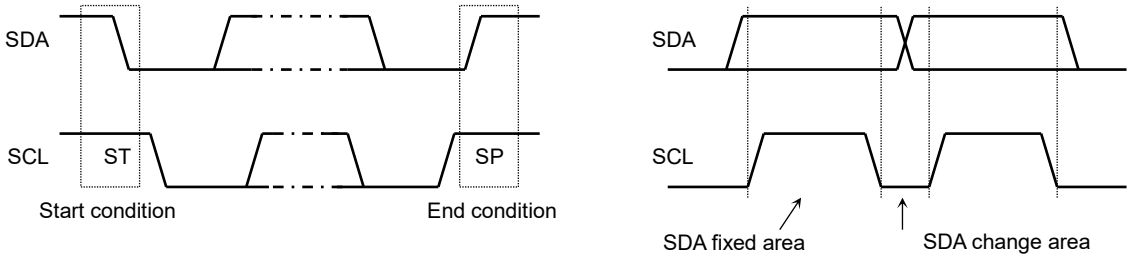

Figure 8.21 Start condition, stop condition, and data communication

- Write procedure of I²C communication
  (1) Start condition
  (2) Slave address of I²C + Write
  (3) Register address
  (4) Write control data
  (5) Stop condition

Table 8.50 I²C communication: SDA minimum data control

S	I²C Slave Address								A	Register Address								A	Control Data								A	P
	A6	A5	A4	A3	A2	A1	A0	R/W		A7	A6	A5	A4	A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0		

- S : Start condition
- A : Acknowledge
- P : Stop condition

- Read procedure of I²C communication
  (1) Start condition
  (2) Slave address of I²C + Write
  (3) Register address
  (4) Start condition
  (5) Slave address of I²C + Read
  (6) Read control data
  (7) Stop condition

8.3.2. NVM Setting

Slave address can be set with ID2 pin and ID1 pin. When both ID2 pin and ID1 pin are set to Low, the slave address can be changed by writing the predetermined slave address to the register.

Table 8.51 Slave address setting

ID2 pin	ID1 pin	Slave address	Note
Low	Low	0101001 (Initial value)	Register 25[7:1]:SLAVE_ADRS It can be stored to NVM.
Low	High	0101001	—
High	Low	0101101	—
High	High	0110010	—

- How to read and write to NVM is as follows.

- **Read procedure of NVM**
  (1) 8'b0000_0000 should be written to the register address:86.
  (2) When 8'b0000_0001 should be written to the register address:87, NVM is started to read.
  (3) Waiting time
  (4) Register address:87 should be read and 8'b0000_0000 is confirmed.

- **Write procedure of NVM**
  (1) 8'b0000_0001 should be written to the register address:86
  (2) When 8'b0000_0001 should be written to the register address:87, NVM is started to read.
  (3) Waiting time
  (4) Register address:87 should be read and 8'b0000_0000 is confirmed.
  * If the write operation is not completed for a certain period,
  (5) 8'b0000_0000 should be written to the register address:87, and the write operation of NVM is forced to end.

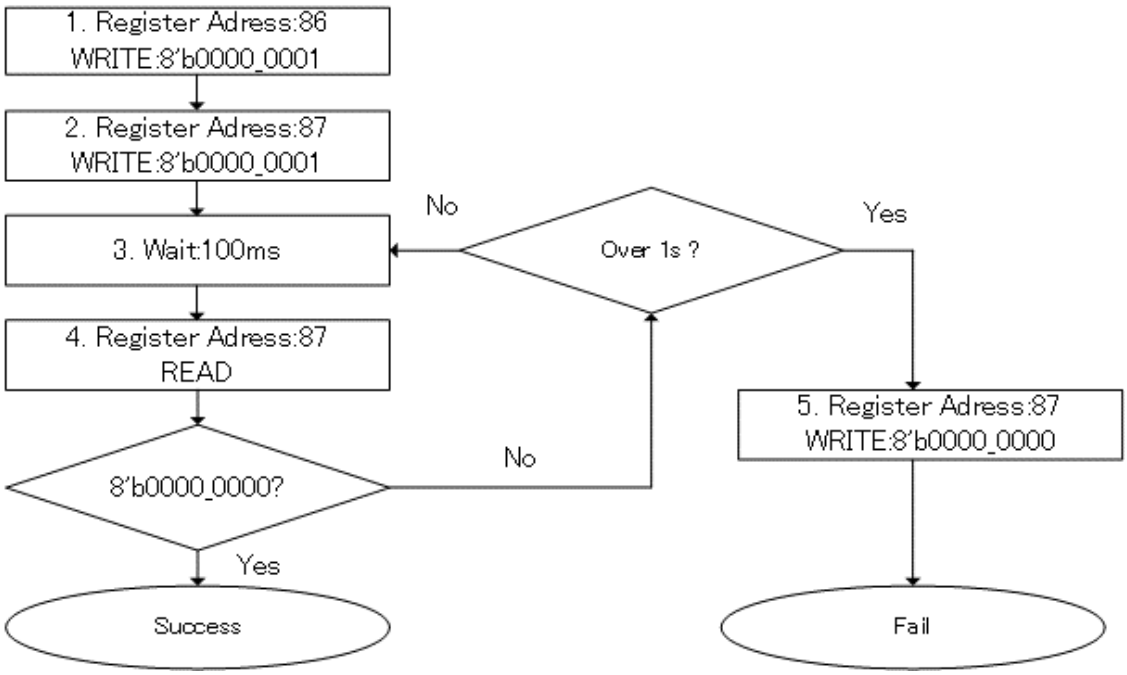

Figure 8.22 Write flow of NVM

8.3.3. Normal Register

Table 8.52 Register map

ADDRESS	Bit	Name	Description	NVM	Read:R Write:W	Initial value
0	7:6	—	—	—	R	0
0	5	CP_LOW	Error state of charge pump voltage drop (0: Normal, 1: Error)	—	R	0
0	4	TSD	Error state of temperature (0: Normal, 1: Error)	—	R	0
0	3	ISD	Error state of over current (0: Normal, 1: Error)	—	R	0
0	2	OV_SPD	Error state of maximum rotation number (0: Normal, 1: Error)	—	R	0
0	1	UD_SPD	Error state of minimum rotation number (0: Normal, 1: Error)	—	R	0
0	0	ST_FAIL	Error state of startup (0: Normal, 1: Error)	—	R	0
1	7:0	USERID	Free	✓	R/W	0
2	7	NOSTOP	No stop mode (0: disable, 1: enable)	✓	R/W	0
2	6:0	STOPDUTY	Stop Duty	✓	R/W	0
3	7:0	STARTDUTY	Start Duty	✓	R/W	0
4	7:0	CHANGEDUTY	Duty of inflection point	✓	R/W	0
5	7:0	MAXDUTY	Max Duty	✓	R/W	0
6	7:0	STARTRPM	Start rotation number	✓	R/W	0
7	7:4	STARTRPM	Start rotation number	✓	R/W	0
7	3:0	MAXDUTYHYS	Hysteresis of Open loop ⇔ Closed loop	✓	R/W	0
8	7:0	SPEEDSLOP	Curve slope	✓	R/W	0
9	7:2	SPEEDSLOP	Curve slope	✓	R/W	0
9	1	MAXOPEN	OPEN control of Max Duty or more (0: disable, 1: enable)	✓	R/W	0
9	0	MAXOFF	Full speed at SPD command OFF (0: disable, 1: enable)	✓	R/W	0
10	7:0	SPEEDSLOP2	Curve slope after inflection point	✓	R/W	0
11	7:2	SPEEDSLOP2	Curve slope after inflection point	✓	R/W	0
11	1	VCP_MASK	Low voltage detection of charge pump (0: enable, 1: disable)	✓	R/W	0
11	0	OPENLOOP	OPEN LOOP/CLOSED LOOP (0: Closed loop, 1: Open loop)	✓	R/W	0
12	7	KIX	KI x 8 (0:1 x, 1:8 x)	✓	R/W	0
12	6:0	KI	KI (0 to 127)	✓	R/W	0
13	7	KPX	KP x 8 (0:1 x, 1:8 x)	✓	R/W	0
13	6:0	KP	KP (0 to 127)	✓	R/W	0
14	7	STBY_MODE	Standby mode	✓	R/W	0
14	6	DIR	Polarity of rotation direction of CWCCW pin (0: positive, 1: negative)	✓	R/W	0
14	5:3	POLEPAIR	Pole number	✓	R/W	0
14	2:1	MAXSPEED	Max speed setting to determine Initial output duty, when the motor rotates from idling.	✓	R/W	0
14	0	FG_ON	FG pin control	✓	R/W	0
15	7:5	FGSEL	Pulse number of FG pin	✓	R/W	0
15	4	TSPSEL	Selection of SPD pin input signal (0: Analog voltage, 1:PWM Duty)	✓	R/W	0
15	3	SPDINV	SPD input polarity (0: positive, 1: negative)	✓	R/W	0
15	2	LATCH	Abnormality detection (0: Auto restart, 1: Latch)	✓	R/W	0
15	1:0	OCPMASK	OCP filter setting	✓	R/W	0
16	7	LOCKDIS	Forced commutation protection (0: enable, 1: disable)	✓	R/W	0
16	6:4	DUTYCHGLIMIT	Limitation of Duty change	✓	R/W	0

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ADDRESS	Bit	Name	Description	NVM	Read:R Write:W	Initial value
16	3:1	STARTCURRENT	Limitation of start current	✓	R/W	0
16	0	OCPDIS	Limitation function of output current (0: enable, 1: disable)	✓	R/W	0
17	7:6	SS_ADD_SEL	Current limitation setting when start current limitation moves to normal current limitation	✓	R/W	0
17	5:4	SS_UP_SEL	Setting of current limitation increasing per 350 ms in SS_ADD_SEL	✓	R/W	0
17	3:1	SS_DUTYCHGLIMIT	Duty limitation at soft start	✓	R/W	0
17	0	DUTY_UP_TIME	Up time of Duty change (0:2.7ms , 1:10.8ms)	✓	R/W	0
18	7:5	RPMLIMIT	Limitation setting of target rotation number change	✓	R/W	0
18	4	BRK_INV	Polarity setting of BRAKE pin (0: positive, 1: negative)	✓	R/W	0
18	3	isd_mask	Over current detection (0: enable, 1: disable)	✓	R/W	0
18	2:1	RS_SEL	Input filter setting of RSA pin	✓	R/W	0
18	0	ANTITHROUGH	Auto Dead time control (0: enable, 1: disable)	✓	R/W	0
19	7:5	WAIT_TIME	Time setting of brake sequence	✓	R/W	0
19	4	WAIT_MODE	Output FET state of brake sequence	✓	R/W	0
19	3	WAIT_CON	Moving state after brake sequence	✓	R/W	0
19	2	LOCK_BRK	Operation settings of minimum rotation count error and start error detection (0: OFF, 1: Short brake)	✓	R/W	0
19	1	alertinv	Polarity of ALERT pin (0: High=Error, 1: Low=Error)	✓	R/W	0
19	0	tsd_mask	Thermal shutdown (0: enable, 1: disable)	✓	R/W	0
20	7:5	TRE	Restart time setting	✓	R/W	0
20	4:3	PreTIP	Setting the first DC excitation time	✓	R/W	0
20	2:0	TIP	Setting the second DC excitation time	✓	R/W	0
21	7:4	LA	Lead angle setting	✓	R/W	0
21	3:2	FMAX	Setting of detection rotation number of maximum rotation speed error	✓	R/W	0
21	1:0	FST	Setting forced commutation frequency	✓	R/W	0
22	7	—	—	✓	R/W	0
22	6:5	—	—	✓	R/W	0
22	4:2	FPWM	Output PWM frequency setting	✓	R/W	0
22	1:0	DEADTIME	Dead time setting	✓	R/W	0
23	7	ISD_LVL	ISD threshold setting (0:1V, 1:0.5V)	✓	R/W	0
23	6	OCP_LVL	Gain settings of output current limitation threshold and output current monitor function	✓	R/W	0
23	5:3	SOURCE	Source current setting of predriver	✓	R/W	0
23	2:0	SINK	Sink current setting of predriver	✓	R/W	0
24	7:6	COMP_HYS	Hysteresis voltage setting of position detection comparator	✓	R/W	0
24	5:0	—	—	✓	R/W	0
25	7:1	SLAVE_ADRS	I^2C Slave address	✓	R/W	0x29
25	0	—	—	✓	R/W	0
26	7:0	—	—	—	R/W	0
27	7:0	SPD	Setting of speed command	—	R/W	0
28	7:6	SPD	Setting of speed command	—	R/W	0
28	5:0	—	—	—	R/W	0
29	7:0	hz_cnt	Rotation frequency	—	R	0
30	7:0	hz_cnt	Rotation frequency	—	R	0

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ADDRESS	Bit	Name	Description	NVM	Read:R Write:W	Initial value
86	7:1	—	—	—	R/W	0
86	0	NVM_W/R	READ/WRITE of NVM (0:READ enable,1:WRITE enable)	—	R/W	0
87	7:1	—	—	—	R/W	0
87	0	NVM_ST	NVM processing (0: Processing end, 1: Processing start)	—	R/W	0

8.4. Abnormality Detection (Error Mode)

8.4.1. Various Abnormality Detection

The abnormality detection functions include power supply low voltage detection, output over current detection, charge pump low voltage detection, thermal shutdown, over maximum speed detection, under minimum speed error detection, and startup failure detection.
When the abnormality state is detected, the IC enters to the error mode. The IC stops operation when power supply low voltage is detected. The output FETs are all off in cases of output over current detection, charge pump low voltage detection, thermal shutdown, and over maximum speed detection. Output FETs are all OFF or short brake depending on the register setting in cases of under minimum speed error detection and startup failure detection. The abnormal detection signal is output with ALART pin.
In error mode, which abnormality detection works can be read from the register by I²C, except UVLO.

Table 8.53 Abnormality detection

Abnormal detection	Read register	Detect condition	Release condition
Power supply low voltage (UVLO)	—	VM < 3.9V or VREG < 3.7V	VM > 4.2 and VREG > 4.0V
Output over current (ISD)	ISD 0[3]	Output current > ISD threshold	・ Output current < ISD threshold *AND* ・ Auto restart after TRE *OR* Release operate
Charge pump low voltage (CPVSD)	CP_LOW 0[5]	VCP - VM < 3.7V	・ VCP-VM > 4.0V *AND* ・ Auto restart after TRE *OR* Release operate
Thermal shutdown (TSD)	TSD 0[4]	Tj > 170°C	・Tj < 130°C *AND* ・ Auto restart after TRE *OR* Release operate
Over maximum speed (FMAX ERROR)	OV_SPD 0[2]	FMAX setting < Current frequency FMAX:0.75kHz/1.5kHz/3kHz/disable	・ Auto restart after TRE *OR* Release operate
Under minimum speed (FMIN ERROR)	UD_SPD 0[1]	FST setting > current frequency FST:1.6Hz/3.2Hz/6.4Hz/12.8Hz	・ Auto restart after TRE *OR* Release operate
Startup failure (STARTUP FAIL)	ST_FAIL 0[0]	Cannot move to sensorless drive mode after force commutation 4 rounds	・ Auto restart after TRE *OR* Release operate

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8.4.2. Recovery from Abnormality Detection

When the abnormality states except UVLO are detected and the IC moves to the error mode, the recovery operation can be selected among auto recovery and latch.
In the auto recovery, IC resumes after moving to the error mode, and restart time elapse. Also, IC resumes with the release operation.
In the latch method, the IC does not resume until the release operation is performed.

- Release operation
  - Speed control command is zero-input.
  - IC moves to standby mode.
  - Power OFF

Table 8.54 Recovery operation setting

Register setting 15[2] LATCH	Recovery operation
0	Auto recovery
1	Latch

Table 8.55 Restart time setting

Register setting 20[7:5] TRE	Restart time (s)
000	0
001	0.5
010	1
011	1.5
100	2
101	4
110	7
111	10

8.4.3. ALERT

The ALERT pin is an open drain type output pin. When an abnormal state is detected, this pin outputs. Output polarity of the ALERT pin can be set.

Table 8.56 Abnormal state polarity setting of ALERT pin

Register setting 19[1] alertinv	Abnormal state
0	High
1	Low

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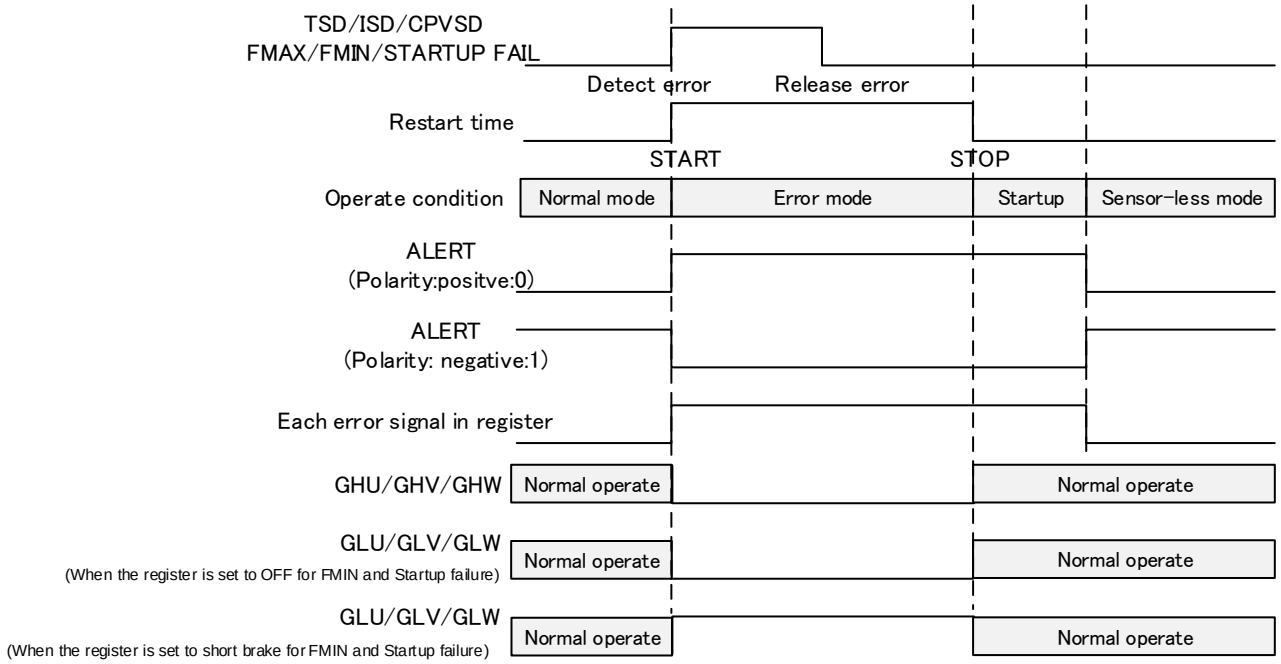

Figure 8.23 Timing chart example of error mode by auto recovery

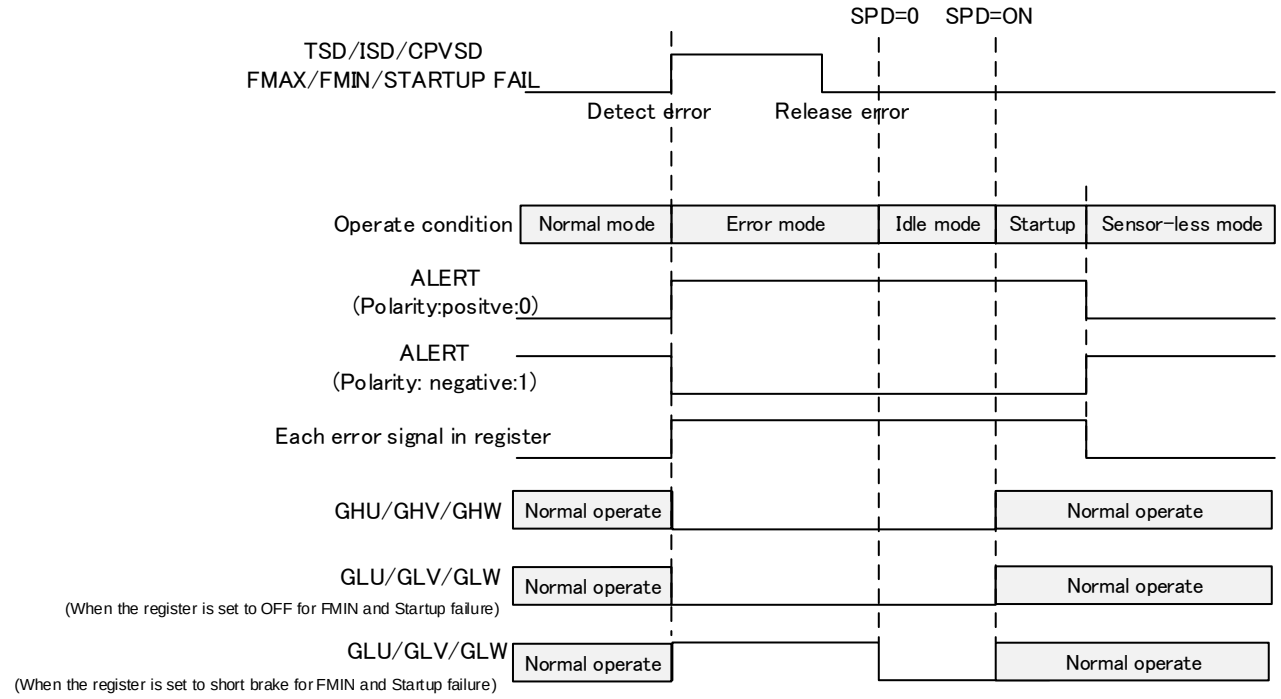

Figure 8.24 Timing chart example of speed command release in error mode by latch method

When the register is set to short brake for FMIN and Startup failure

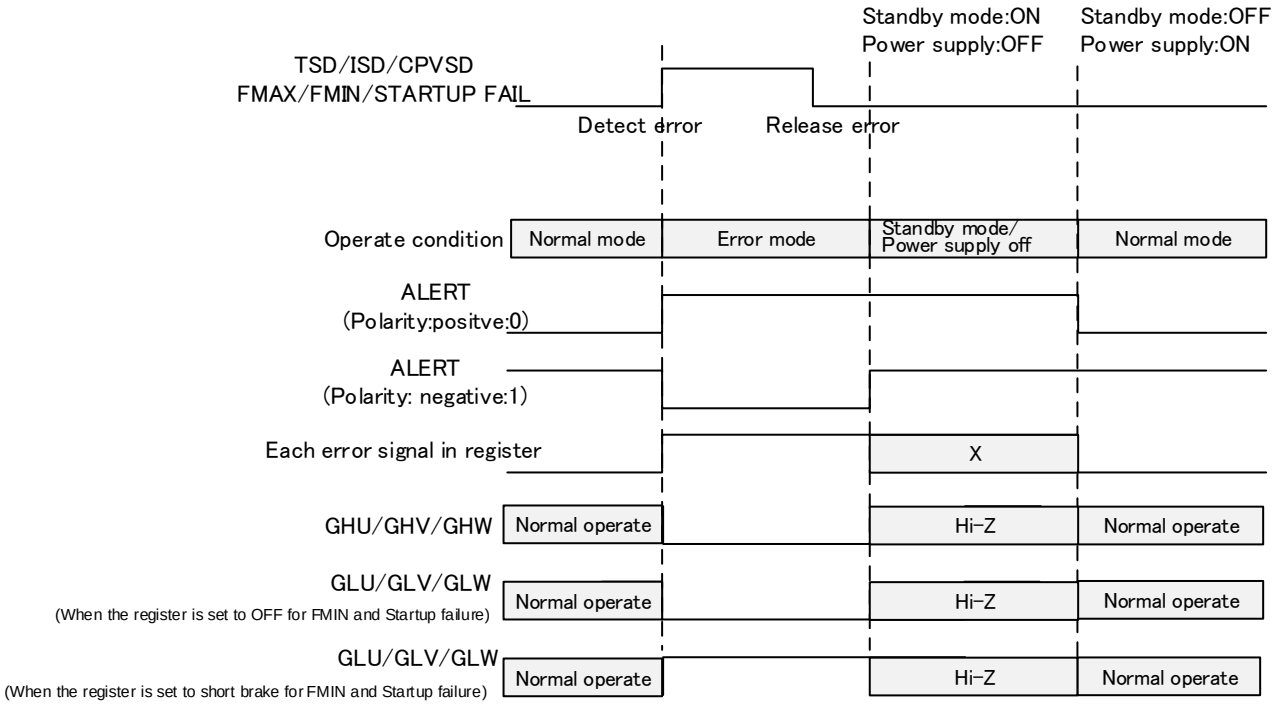

Figure 8.25 Timing chart example of standby mode / power off release in error mode by latch method

8.4.4. Max Rotation Count Error, Minimum Rotation Count Error, and Start Error

In the max rotation count error, when the motor rotation count reaches the maximum rotation frequency setting or more, the IC moves to the error mode, and external FET outputs are all turned off.

In the minimum rotation count error, when the rotation count of the motor falls to below the forced commutation frequency, the IC moves to the error mode. The operation at detecting can be selected among external FETs all OFF, and short brake setting.

In the start error, if the motor rotates four times with forced commutation, and the IC does not move to the sensorless drive, it moves to error mode. The operation at detecting can be selected among all off setting of the external FETs and the short brake setting.

When the motor is locked, the motor cannot be rotated. Therefore, the IC detects the minimum rotation count error or start error, and moves to the error mode.

Table 8.57 Max rotation frequency (max rotation count or more) setting

Register setting 21[3:2] FMAX	Max rotation frequency
00	0.75 kHz
01	1.5 kHz
10	3 kHz
11	None

Table 8.58 Forced commutation frequency (minimum rotation count error) setting

Register setting 21[1:0] FST	Electrical angle frequency	Idling detection time (electrical angle frequency)
00	1.6 Hz	200 ms (5 Hz)
01	3.2 Hz	100 ms (10 Hz)
10	6.4 Hz	50 ms (20 Hz)
11	12.8 Hz	25 ms (40 Hz)

- The forced commutation frequency is same as the detection frequency of minimum rotation count error, and changes with idling detection time.

Table 8.59 Operation settings of minimum rotation count error and start error detection

Register setting 19[2] LOCK_BRK	Operation
0	Output FET all OFF
1	Output FET short brake

Table 8.60 Enable / disable setting of start error function

Register setting 16[7] LOCKDIS	Start error function
0	Enable
1	Disable

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8.4.5. Under Voltage Lockout Detection (UVLO)

When the power supply voltage is less than the IC operating voltage, this function turns off the IC operation to avoid malfunction.
It monitors both VM voltage and VREG voltage. When VM voltage is 3.9 V (typ.) or less, or VREG voltage is 3.7 V (typ.) or less, this function is activated. It has a hysteresis of 0.3 V (typ.). IC is resumed to normal operation when VM voltage is over 4.2 V (typ.), and VREG voltage is over 4.0 V (typ.).

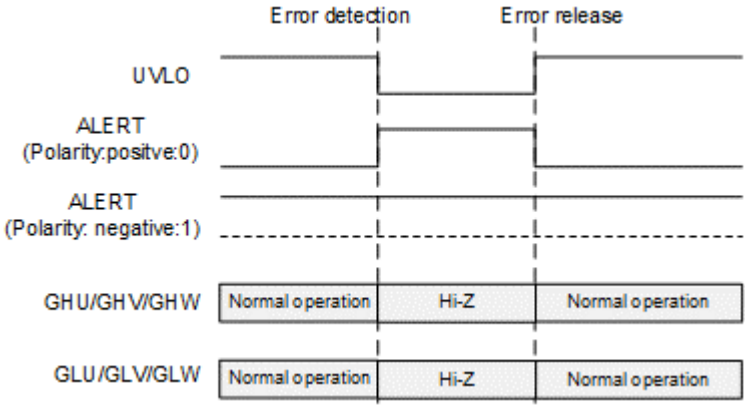

Figure 8.26 Timing chart example of UVLO operation

8.4.6. Output Over Current Detection (ISD)

To prevent the IC from flowing over current continuously, the motor current is detected with external shunt resistor. The detected voltage that is input to RSA pin becomes ISD reference voltage VISD or more, the external FET outputs are all OFF.

Table 8.61 ISD reference voltage setting

Register setting 23[7] ISD_LVL	ISD reference voltage VISD
0	1V
1	0.5V

Table 8.62 Enable / disable setting of ISD function

Register setting 18[3] isd_mask	ISD function
0	Enable
1	Disable

8.4.7. Low Voltage Detection for Charge Pump (CPVSD)

When the voltage between VCP and VM is 3.7 V(typ.) or less, motor outputs are turned off (as high impedance state). It has a hysteresis of 0.3 V (typ.). Motor is resumed to the normal operation when the voltage difference is over 4.0 V (typ.).

Table 8.63 Enable / disable setting of CPVSD function

Register setting 11[1] VCP_MASK	CPVSD function
0	Enable
1	Disable

8.4.8. Thermal Shutdown

Thermal shutdown (TSD) is incorporated.
It operates when IC's junction temperature (Tj) exceeds 170°C (typ.). All output FETs are turned off. It has a hysteresis of 40°C (typ.). When IC's junction temperature becomes 130°C (typ.) or less, the operation returns automatically.

Table 8.64 Enable / disable setting of TSD function

Register setting 19[0] tsd_mask	TSD function
0	Enable
1	Disable

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9. Absolute Maximum Ratings

Table 9.1 Absolute Maximum Ratings(Unless otherwise specified, Ta=25°C)

Characteristics	Symbol	Rating	Unit	Remarks
Motor power supply voltage	VMvmax	30	V	VM
5V reference voltage	VREGvmax	6 (Note1)	V	VREG
Charge pump voltage	VCPvmax	VM+10 (Note 1)	V	VCP
	VCPMvmax	VM	V	CPM
	VCPPvmax	VM+10	V	CPP
Input voltage	Vmaxin1	-0.3 to 6	V	STBY/SPD/SEL/ID1/ID2/SCL/SDA/CW CCW/BRAKE/TESTI/TESTO
	Vmaxin2	30	V	OUTU/OUTV/OUTW
	Vmaxin3	6	V	RSA/RSB
Output voltage	Vmaxo1	18	V	GLU/GLV/GLW
	Vmaxo2	6	V	ALERT/FG/PHBF/PH
	Vmaxo3	VM+10	V	GHU/GHV/GHW
Output current	Imax1	10	mA	ALERT/FG
	Imax2	-120	mA	GHU/GHV/GHW/GLU/GLV/GHW
	Imax3	240	mA	GHU/GHV/GHW/GLU/GLV/GHW
	Imax4	2	mA	PHBF
	Imax5	30	mA	VREG
Power dissipation	P_D	4.1	W	Mounted on a board (4-layer board: FR4:76.2 mm x 114.3 mm x 1.6 mm), Rth (j-a) = 30.5°C/W
Operating temperature	Topr	-40 to 105	°C	—
Storage temperature	Tstg	-55 to 150	°C	—
Junction temperature	Tjmax	150	°C	—

Note 1: VREG and VCP pin voltages are generated in the IC. Do not apply voltage externally.
Note 2: Output current may be restricted by ambient temperature and the mounting board. Please design not to exceed the junction temperature.

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
Please use this IC within the specified operating ranges.

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10. Operating Range

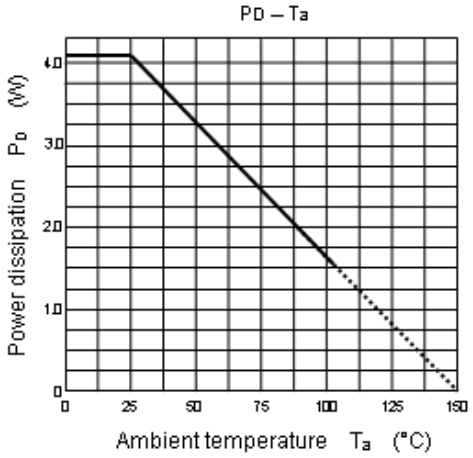
Table 10.1 Operating range (Unless otherwise specified, Ta=-40 to 105°C)

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
VM pin power supply voltage 1	$V_{M(opr1)}$	9	14.8	27	V	
VM pin power supply voltage 2	$V_{M(opr2)}$	5.5	—	9	V	Electrical characteristics are only for reference because the variation of electrical characteristics becomes large
VM pin power supply voltage 3	$V_{M(opr3)}$	10.8	14.8	27	V	For NVM writing
Input PWM command frequency	f_{TSP}	1	—	100	kHz	—
Input I^2C CLK frequency	f_{SCK}	—	—	400	kHz	—

Table 10.2 NVM characteristics

Characteristics	Conditions	Min	Max	Unit
Program/Erase cycles	T_j=0 to 90°C	10	—	Cycle

10.1. Power Dissipation



Mounted on a board (4-layer board: FR4:76.2 mm x 114.3 mm x 1.6 mm), Rth (j-a) = 30.5°C/W

Figure 10.1 Power dissipation

11. Electrical Characteristics

Table 11.1 Electrical Characteristics (Unless otherwise specified, VM = 14.8V, Ta = 25°C)

Pin / Circuit	Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
VM	Power supply current 1	I_{VM1}	Idle mode	—	15	18	mA
	Power supply current 2	I_{VM2STB}	Standby mode STBY=0V	—	0	10	μA
	UVLO operating voltage	V_{UVOVM}	In VM falling	3.7	3.9	4.1	V
	UVLO hysteresis voltage	V_{UVHYVM}	—	—	300	—	mV
	UVLO release voltage	V_{UVRVM}	In VM rising	4.0	4.2	4.4	V
VREG	5V reference voltage	V_{VREG}	Iout=0mA	4.75	5.0	5.35	V
	5V reference at voltage output current	V_{IVREG}	Iout =-10mA	4.75	5.0	5.35	V
	UVLO operating voltage	$V_{UVOVREG}$	In VREG falling	3.5	3.7	3.9	V
	UVLO hysteresis voltage	$V_{UVHYVREG}$	—	—	300	—	mV
	UVLO release voltage	$V_{UVRVREG}$	In VREG rising	3.8	4.0	4.2	V
VCP	Charge pump voltage	V_{VCP}	VM=9V: Idle mode Between VM and VCP pins: 0.1μF, Between CPP and CPM pins: 0.01μF	VM + 7.5	VM + 8	VM + 8.5	V
	CPVSD operating voltage	V_{CPVSDO}	In the voltage between VM pin and VCP pin falling, VM ≥ 5.5V	3.4	3.7	4.0	V
	CPVSD hysteresis voltage	$V_{CPVSDHY}$	—	—	300	—	mV
	CPVSD release voltage	V_{CPVSDR}	In the voltage between VM pin and VCP pin rising. VM ≥ 5.5V	3.7	4.0	4.3	V
GHU, GHV, GHW	Output H voltage	V_{OHGHX}	Iout = -1mA	VCP – 1.5	VCP – 0.3	VCP	V
	Output L voltage	V_{OLGHX}	Iout = 1mA	—	0.3	0.8	V
	Output source current 1	I_{SOGHX1}	—	-12	-10	-8	mA
	Output source current 2	I_{SOGHX2}	—	-120	-100	-80	mA
	Output sink current 1	I_{SIGHX1}	—	16	20	24	mA
	Output sink current 2	I_{SIGHX2}	—	160	200	240	mA
GLU, GLV, GLW	Output H voltage	V_{OHGLX}	Iout= -1mA	6.9	7.7	8.5	V
	Output L voltage	V_{OLGLX}	Iout = 1mA	—	0.05	0.2	V
	Output source current 1	I_{SOGLX1}	—	-12	-10	-8	mA
	Output source current 2	I_{SOGLX2}	—	-120	-100	-80	mA
	Output sink current 1	I_{SIGLX1}	—	16	20	24	mA
	Output sink current 2	I_{SIGLX2}	—	160	200	240	mA
OUTU, OUTV, OUTW	Comparator offset voltage	$V_{COFSOUTX}$	(Reference value)	-1	0	1	mV
	Comparator hysteresis voltage 1	$V_{CHYOUTX1}$	(Reference value)	±40	±100	±150	mV
	Comparator hysteresis voltage 2	$V_{CHYOUTX2}$	(Reference value)	±80	±200	±300	mV
	Comparator hysteresis voltage 3	$V_{CHYOUTX3}$	(Reference value)	±120	±300	±450	mV
STBY	Input H voltage	V_{IHSTB}	—	2.0	—	5.5	V
	Input L voltage	V_{ILSTB}	—	-0.3	—	0.8	V
	Hysteresis voltage	V_{HYSTB}	—	—	200	—	mV
	H input current	I_{IHSTB}	Vin=5V	17	25	33	μA
	L input current	I_{ILSTB}	Vin=0V	—	—	1	μA
	Standby mode setting time	T_{SETSTB}	STBY:H to L	95	100	105	ms

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Pin / Circuit	Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
SPD (during digital signal input)	Input H voltage	V_{IHSPD}	—	2.0	—	5.5	V
	Input L voltage	V_{ILSPD}	—	-0.3	—	0.8	V
	Hysteresis voltage	V_{HYSPD}	—	—	200	—	mV
	H input current	I_{IHSPD}	Vin=5V	—	—	1	μA
	L input current	I_{ILSPD}	Vin=0V	—	—	1	μA
	Input frequency	f_{ISPD}	—	1	—	100	kHz
	100%Duty detection time	t_{100SPD}	—	—	1.5	—	ms
	0%Duty detection time	t_{0SPD}	—	—	100	—	ms
SPD (during analog voltage input)	100% input voltage	V_{100SPD}	ADC = 512 (100%)	3.9	4.0	4.1	V
	0% input voltage	V_{0SPD}	ADC = 0(%)	1.4	1.5	1.6	V
CWCCW	Input H voltage	V_{IHCW}	—	2.0	—	5.5	V
	Input L voltage	V_{ILCW}	—	-0.3	—	0.8	V
	Hysteresis voltage	V_{HYCW}	—	—	400	—	mV
	H input current	I_{IHCW}	Vin=5V	70	100	130	μA
	L input current	I_{ILCW}	Vin=0V	—	—	1	μA
BRAKE	Input H voltage	V_{IHCW}	—	2.0	—	5.5	V
	Input L voltage	V_{ILCW}	—	-0.3	—	0.8	V
	Hysteresis voltage	V_{HYCW}	—	—	400	—	mV
	H input current	I_{IHCW}	Vin=5V	70	100	130	μA
	L input current	I_{ILCW}	Vin=0V	—	—	1	μA
SEL	Input H voltage	V_{IHSEL}	—	2.0	—	5.5	V
	Input L voltage	V_{ILSEL}	—	-0.3	—	0.8	V
	Hysteresis voltage	V_{HYSEL}	—	—	400	—	mV
	H input current	I_{IHSEL}	Vin=5V	70	100	130	μA
	L input current	I_{ILSEL}	Vin=0V	—	—	1	μA
FG	Output L voltage	V_{LFG}	Iout=5mA	—	0.15	0.30	V
	Output leakage current	I_{LFG}	Vout=6V	—	—	1	μA
ALERT	Output L voltage	V_{LALERT}	Iout=5mA	—	0.15	0.30	V
	Output leakage current	I_{LALERT}	Vout=6V	—	—	1.0	μA
RSA	Output current limit reference voltage 1	V_{OCP1}	0.25V setting	0.225	0.25	0.275	V
	Output current limit reference voltage 2	V_{OCP2}	0.125V setting	0.113	0.125	0.137	V
	Over current reference voltage 1	V_{ISD1}	0.5V setting	0.45	0.5	0.55	V
	Over current reference voltage 2	V_{ISD2}	1V setting	0.9	1	1.1	V
	Input current	I_{IRSA}	RSA=0V	—	0.1	1	μA
RSB	Input current1	I_{IRSB1}	Vin=5V, Gain=10	35	45	65	μA
	Input current2	I_{IRSB2}	Vin=5V, Gain=20	18	24	35	μA
PH	Output H voltage	V_{OHPH}	—	VREG-1.2	VREG-0.85	VREG	V
	Output L voltage	V_{OLPH}	—	0	0	0.1	V
	Output voltage 1	V_{OPH1}	Gain=10, RSB=0.25V	2.4	2.5	2.6	V
	Output voltage 2	V_{OPH2}	Gain=20, RSB=0.125V	2.4	2.5	2.6	V

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Pin / Circuit	Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
	Output current 1	I_{OPH1}	Gain=20, RSB=0.125V, PH=2.4V	400	840	1400	μA
	Output current 2	I_{OPH2}	Gain=20, RSB=0.125V, PH=2.6V	0	0	1.0	μA
PHBF	**Output H voltage**	V_{OHPHBF}	—	VREG-1.2	VREG-0.85	VREG	V
	Output L voltage	V_{OLPHBF}	—	0	0	0.1	V
	Output voltage 1	V_{OPHBF1}	Gain=10, RSB=0.25V	2.4	2.5	2.6	V
	Output voltage 2	V_{OPHBF2}	Gain=20, RSB=0.125V	2.4	2.5	2.6	V
	Output voltage 3	V_{OPHBF3}	Gain=20, RSB=0.125V, PHBF=2mA	2.4	2.53	2.75	V
	Output voltage 4	V_{OPHBF4}	Gain=20, RSB=0.125V, PHBF=-2mA	2.25	2.48	2.6	V
Internal circuit	**OSC frequency**	f_{OSC}	—	11.64	12.00	12.36	MHz
	Output PWM frequency 1	f_{OPWM1}	FPWM = 000	—	23.4	—	kHz
	Output PWM frequency 2	f_{OPWM2}	FPWM = 011	—	187.5	—	kHz
TSD	**Shutdown temperature**	T_{TSD}	In rising temperature (Reference value)	—	170	—	°C
	Release hysteresis temperature	T_{HYTSD}	(Reference value)	—	40	—	°C
	Shutdown release temperature	T_{RTSD}	In falling temperature (Reference value)	—	130	—	°C
ID1 ID2	**Input H voltage**	V_{IHIDX}	—	2.0	—	5.5	V
	Input L voltage	V_{ILIDX}	—	-0.3	—	0.8	V
	Hysteresis voltage	V_{HYIDX}	—	—	400	—	mV
	H input current	I_{IHIDX}	—	70	100	130	μA
	L input current	I_{ILIDX}	—	—	—	1	μA
SDA SCL	**Input H voltage**	V_{IHI2C}	—	2.0	—	5.5	V
	Input L voltage	V_{ILI2C}	—	-0.3	—	0.8	V
	Hysteresis voltage	V_{IHYI2C}	—	—	400	—	mV
	Input current	I_{II2C}	Vin=0V to 5V	-5	1	5	μA
	SDA Output L voltage	V_{OLSDA}	Iout=6mA	—	—	0.4	V
	SDA Output leakage current	I_{LSDA}	Vout=6V	—	—	1	μA
	SCL clock frequency	f_{SCL}	—	—	—	400	kHz
	Hold time Start condition	t_{HDSTA}	—	0.6	—	—	μs
	Setup time Start condition	t_{SUSTA}	—	0.6	—	—	μs
	SCL clock Low period	t_{LOW}	—	1.3	—	—	μs
	SCL clock High period	t_{HIGH}	—	0.6	—	—	μs
	Data hold time	t_{HDDAT}	—	0	—	—	ns
	Data setup time	t_{SUDAT}	—	100	—		ns
	Setup time Stop condition	t_{SUSTO}	—	0.6	—	—	μs
	Bus free time Stop / start condition	t_{BUF}	—	1.3	—	—	μs

Reference value: It means a design value. The test before shipment has not been performed.

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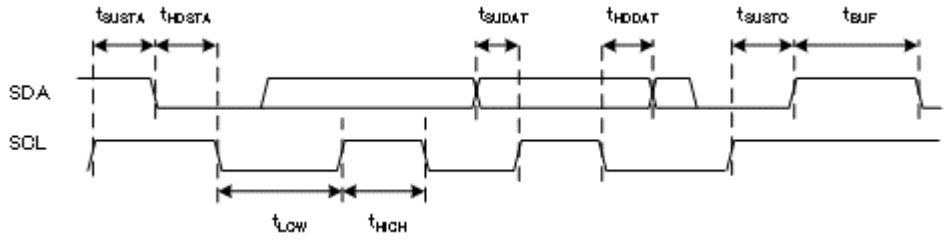
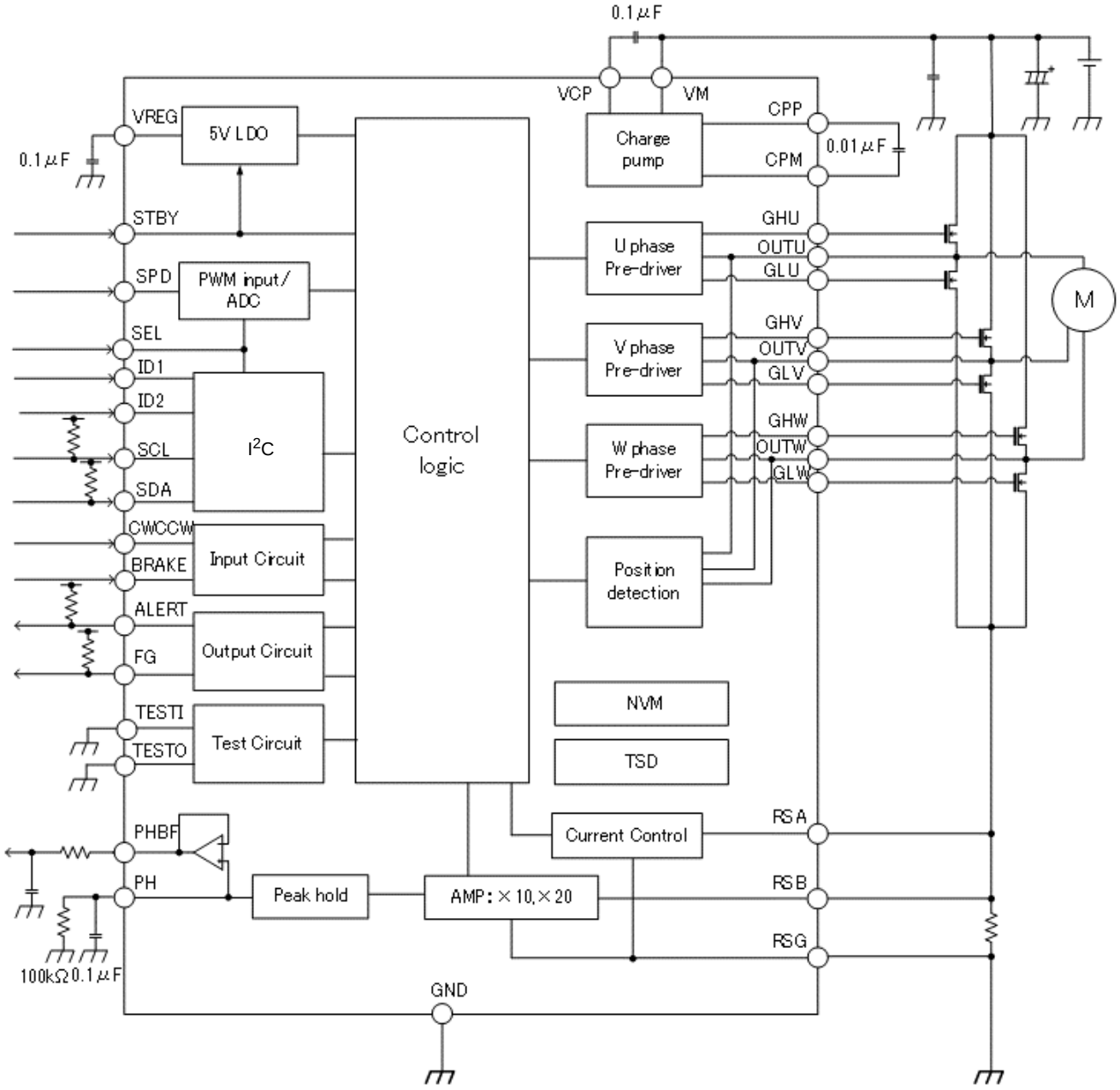


Figure 11.1 Electrical characteristics of I^2C timing chart

12. Example of Application Circuit

Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.



Note: As for the external FET, the specification whose gate threshold voltage is minimum 1.0V at Ta 25 °C is recommended.

13. Package Dimensions

P-WQFN36-0505-0.50-001 "Unit:mm"

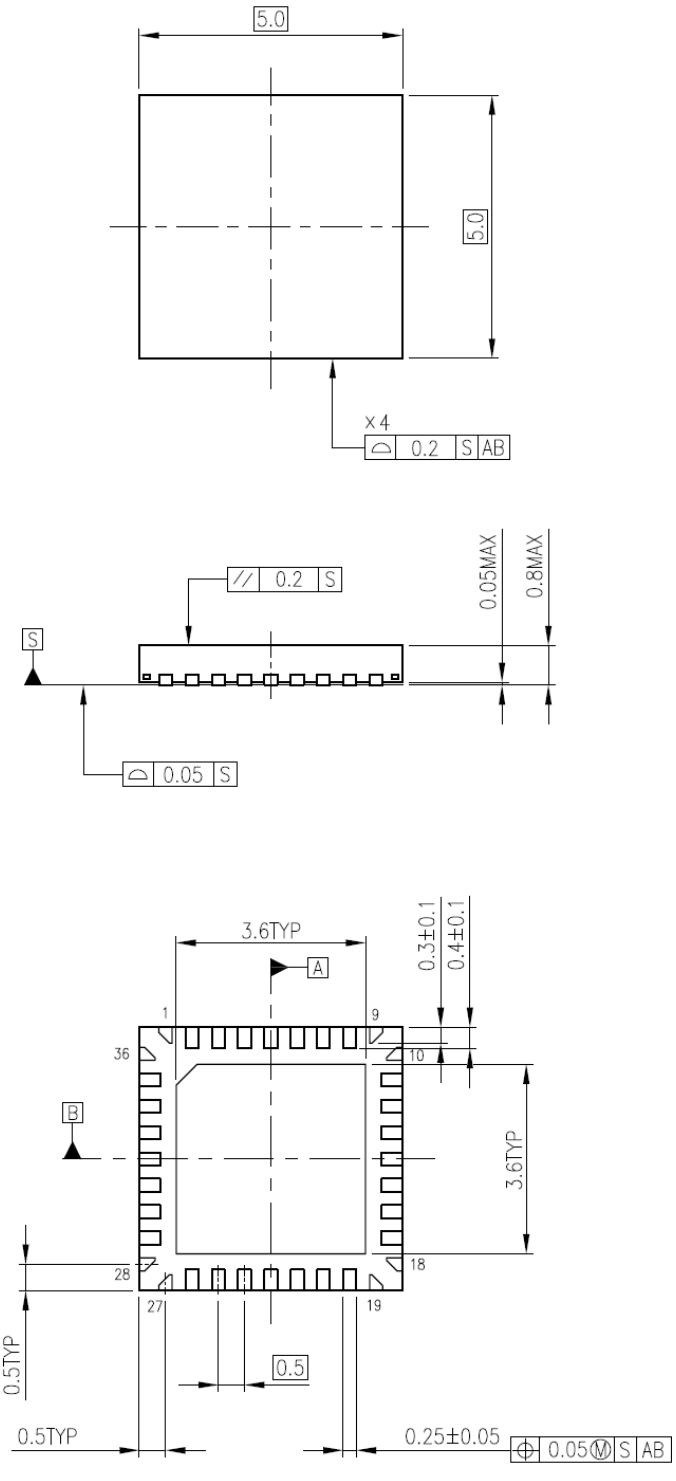


Figure 13.1 Package Dimensions

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

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Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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